

Nonconformance Report



**Solar Orbiter
Energetic Particles
Detector (EPD)**
EPT-HET ☒ STEP ☐

NCR-N°: ____0016____ Revision ____
Related internal NCR-No.: ____
Critical Item: Yes ☒ No ☐
Page 1 of _11_ Attachments: ____

NCR Title **SO-EPD-KIE-NC-0016 post Vib FT anomalies**

NC Item Identification **EPT-HET**

Name: Sr-N: CI-No.:

Drawing No.

Next higher Assembly **EPD**

Procedure No.

Subsystem

Model . **PQM**

Supplier: **CAU Kiel**

NC Observation

Date: **2015-05-20** Location: **Portsmouth ADS Facilities**

NC detected during: **Test, after Z-axis qual random**

Description of Nonconformance

After an apparently nominal start to data acquisition at 10:57 during the functional test after completing the qualification vibration test, the input current was observed to change to 240mA from the nominal 180mA. During the following 20 minutes this current gradually reduced to 190mA, but it was found that all eight EPT channels and both HET channels were excessively noisy. Data acquisition was stopped and the instrument powered off at 11:48. A subsequent power on was stopped almost immediately when current fluctuations (160-210mA) were observed. Post test quick analysis of HK showed a short dropout of Vbias, and a later gradual decrease of shaper Vcc and HET Vfet. Before performing the FT a nominal impedance check had been carried out.

Requirements violated:

Initiator: Date, Name and Signature
2015-05-20, S.Kulrarni

Internal NRB Dispositions:

Ref. to MoMs attached, PQM EPT-HET Non Conformance Review Board, 29 May and 01 June.

Classification:

Minor ☐ Major ☒

Fault analysis was carried out as summarised in annex.
Hardware was inspected at CAU Kiel. Damage to LVPS, Digital and Analog boards is itemised in attachment.
Telecom with OHB confirmed parts and gluing damage.

Customer Notification per email

Cause of NC: Excessive bending under vibration, cause of strength of resonance to be investigated

Corrective/Preventive Actions:
PQM EPT-HET – rework for thermal test, but no further qualification
PQM STEP – RFD (td) for notching resonance and to lower random vibration levels

Verification: Test

Ref to Failure Report

Date:
Name:
Signature:

PA

Mr. Richard

Engineering

S.Kulrarni

Customer NRB Dispositions (Class major, only)

Ref. to MoMs

Verification

Finally determined Cause of NC

Corrective/Preventive Actions

Ref to Failure Report

Request for Waiver No ☐ Yes ☐

Alert No ☐ Yes ☐

Other related Documents

Reference:

Reference

NRB Approval
Organization/Name

Chairman

NCR Close out

Date, Signature, Stamp

Nonconformance Report		
<div><div>C A U</div><div>ieap</div><div>Christian-Albrechts-Universität zu Kiel</div></div>	<div>Solar Orbiter Energetic Particles Detector (EPD) EPT-HET <input checked="" type="checkbox"/> STEP <input type="checkbox"/></div>	<div>NCR-N°: ____0016____ Revision ____ Related internal NCR-No.: ____ Critical Item: Yes <input checked="" type="checkbox"/> No <input type="checkbox"/> Page 2 of _11 Attachments: _____</div>

Date, Signature						
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NCR Title: SO-EPD-KIE-NC-0016

- Continuation Sheet -

NCR Treatment Sequence / Findings / Statements / Actions		Verification
<p>The first analysis of housekeeping was made at ADS Portsmouth environmental test facility immediately after the failure was observed. The following graphic shows a dropout in temperature sensors at HET Sensors 1 & 2, as well as bias voltage and current.</p> <div><p>HET/EPT HK: data/2015-05-20-10-57-post-vibration.HK</p><p>Summary of EPT-HET PQM fault analysis</p><p>(1) Email Bjoern Schuster</p><p>short summery from my side of the todays "autopsy".</p><p>The LVPS had sporadic errors in output voltages when pressing on PCB or by twisting the board, which let me believe to a broken solder connection. The behavior of the output voltages points to an error in the signal path on the primary side. And that is it, where the error was found.</p></div>		

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The LVPS has multiple cracks in pins of different parts. Two cracked pins of the PWM generator seems to be the reasons for the falling analog voltage during vibration.

One of the two cracked pins is the feedback input for PWM generator.

There are some more cracks I have found and I believe that there will be some more.

The cracks at PWM generator I have found because I had the strong suspicion that there is the source of error, so I have inspected this part very detailed.

I will fix this error tomorrow. But the parts on board are very stressed now and won't survive a second vibration test.

I don't believe that the LVPS is the reason for failure in the FPGA IO bank. We will see on tomorrow.

The attachment had six photos and assembly diagrams for location:

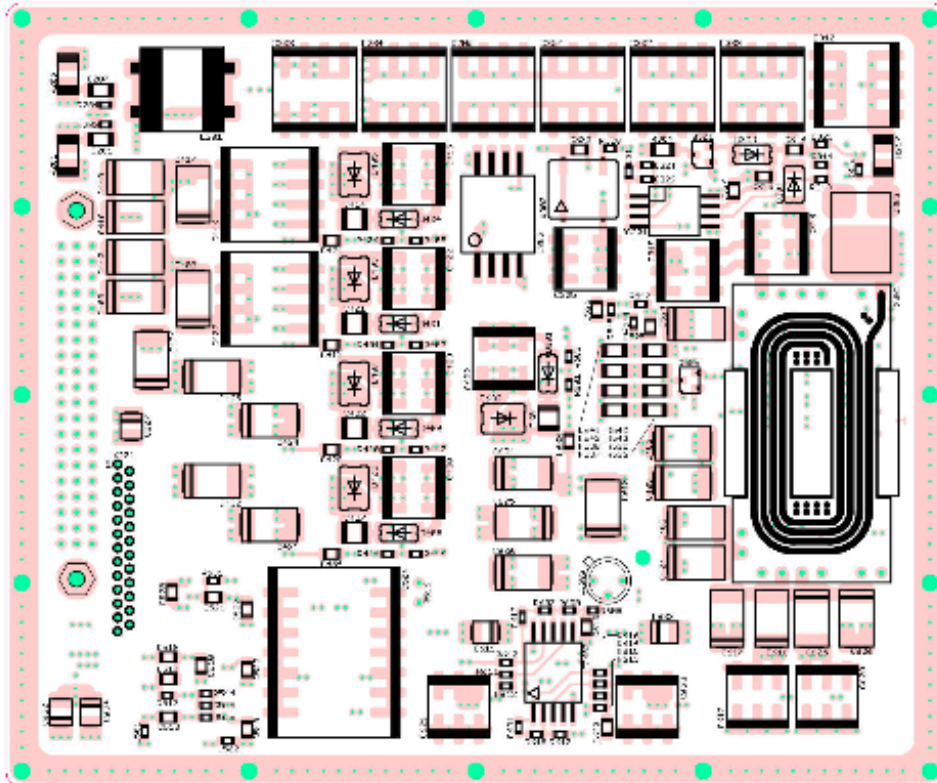


Abb 1 Assembly top

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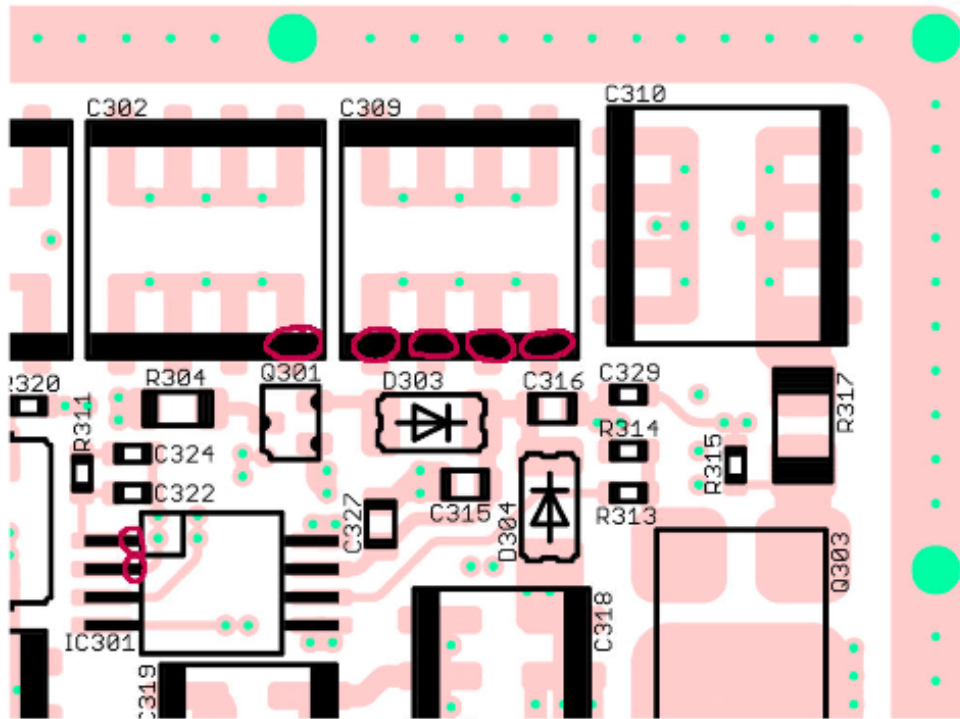


Abb 2 Assembly top detail

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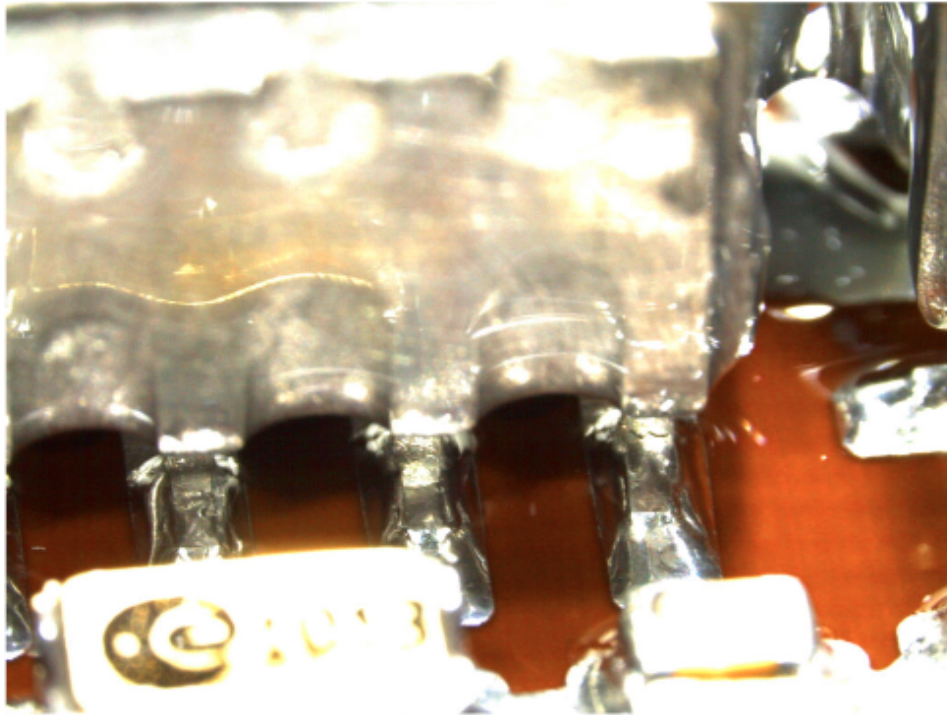


Abb 3 Crack at Capacitor C309

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Abb 4 Crack at Capacitor C309 detail

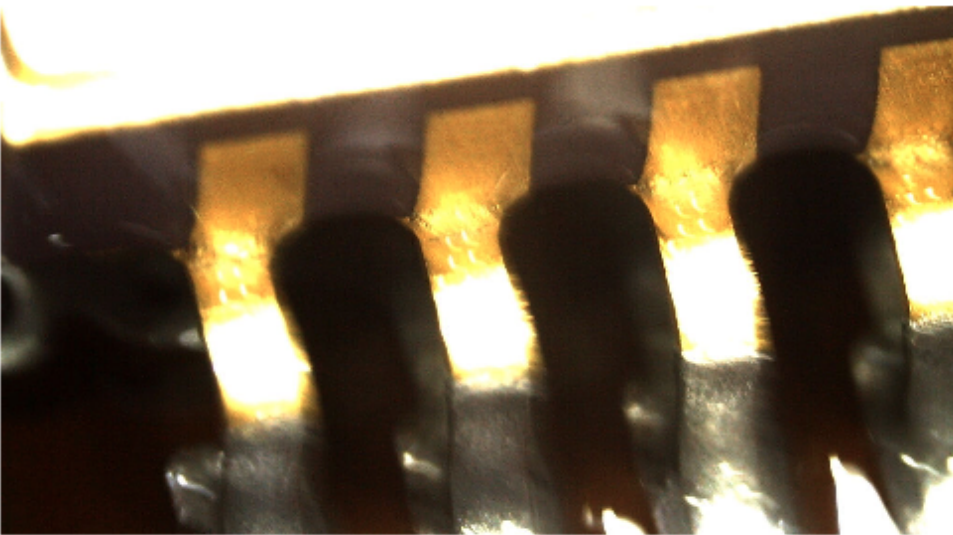


Abb 5 Crack on Pin 1 & at IC301

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Abb 6 Crack on Pin 1 &2 at IC301 detail 01

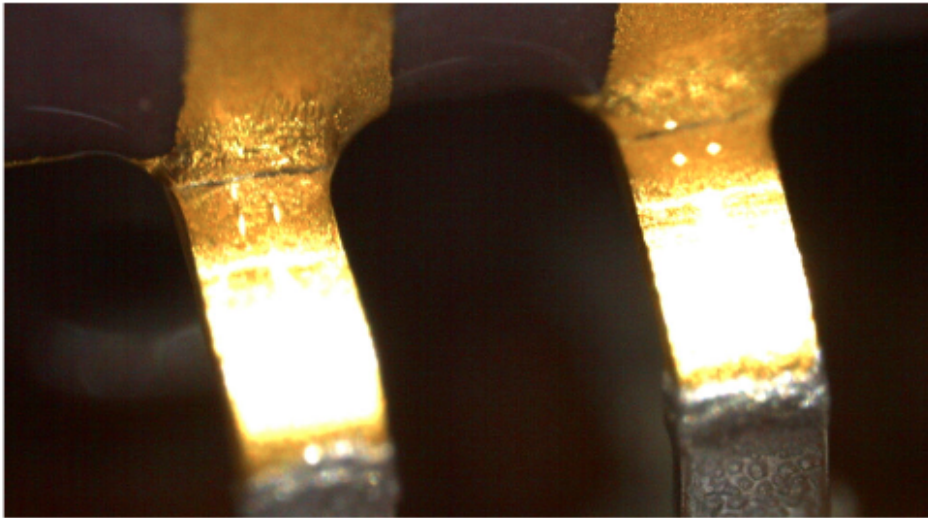


Abb 7 Crack on Pin 1 &2 at IC301 detail 02

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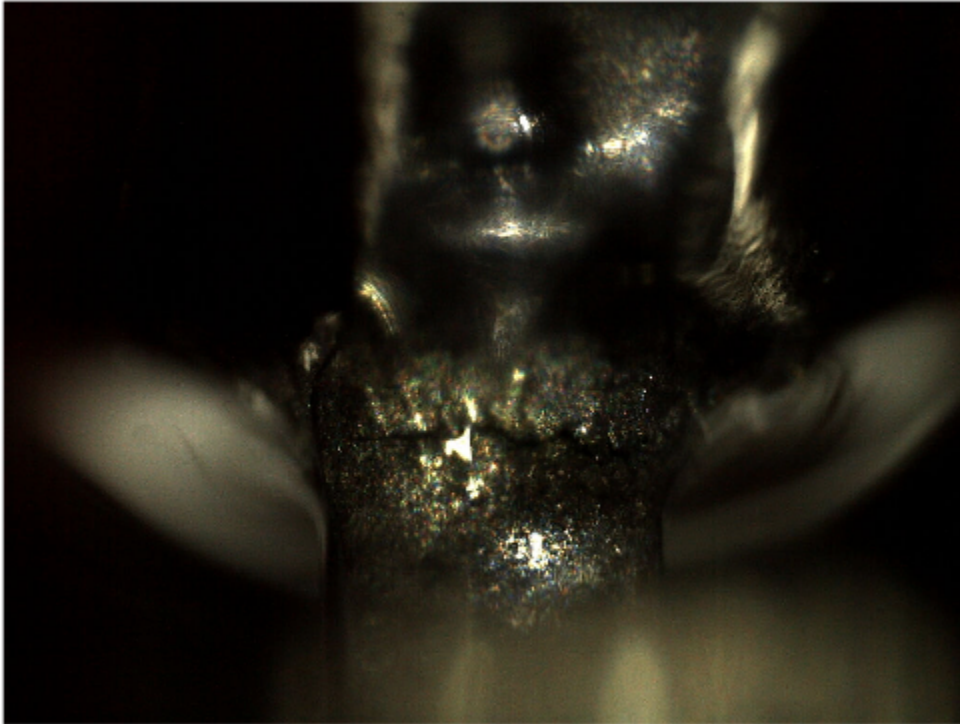


Abb 8 Crack at Capacitor C302

(2) On 2015-05-28 Shri Kulkarni posted his investigation of the Analog board. Cracks were observed in FPGA legs, as indicated in the sketched assembly diagram, and documented by photos.

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Analog PQM Board

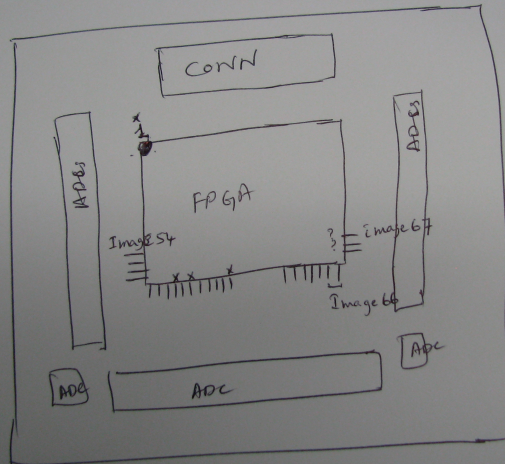
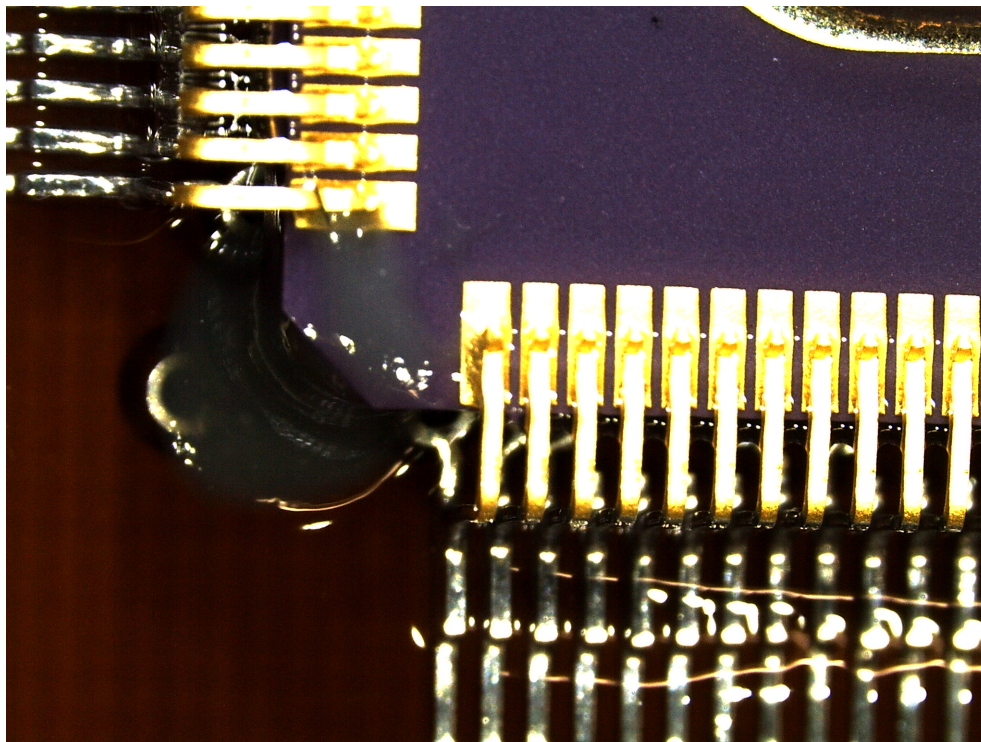


Image 54 to Image 67



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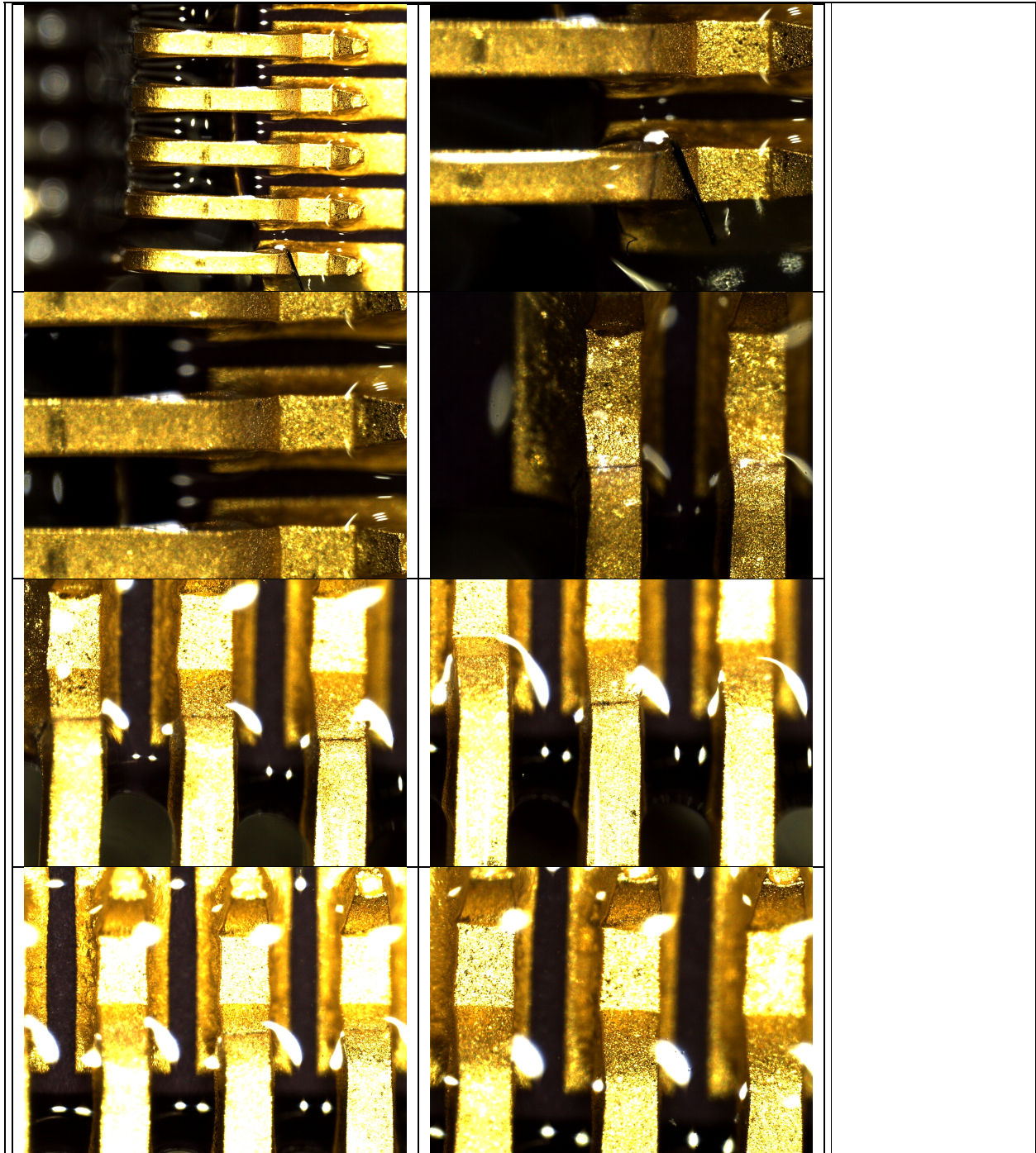
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EPT-HET ☒ **STEP** ☐

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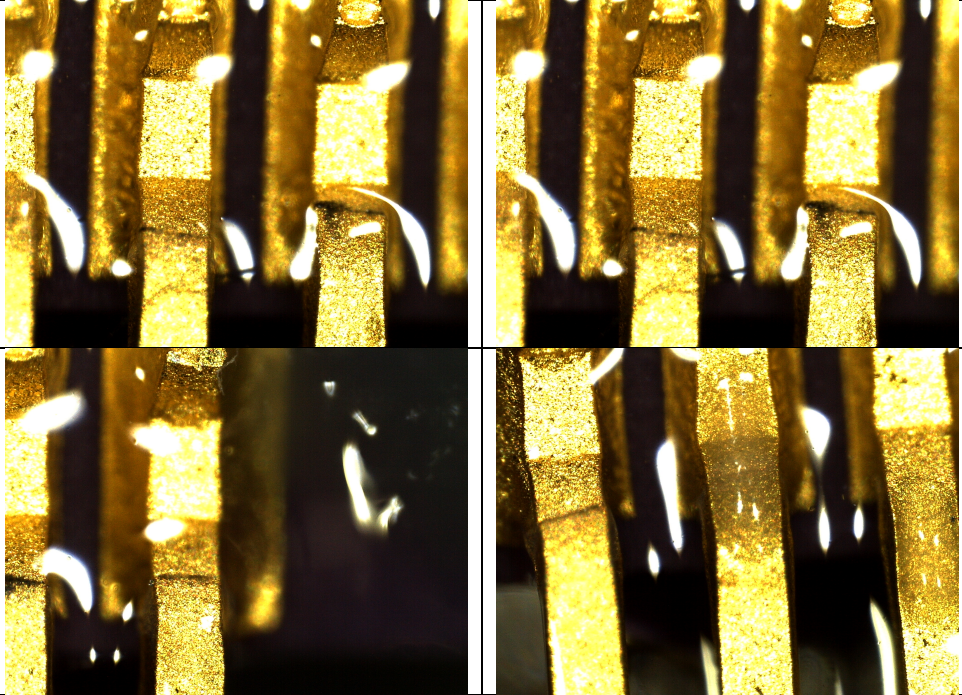
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(3) Successful test of EPT sensor head, email S. Kulkarni, 2015-05-29

Test setup:

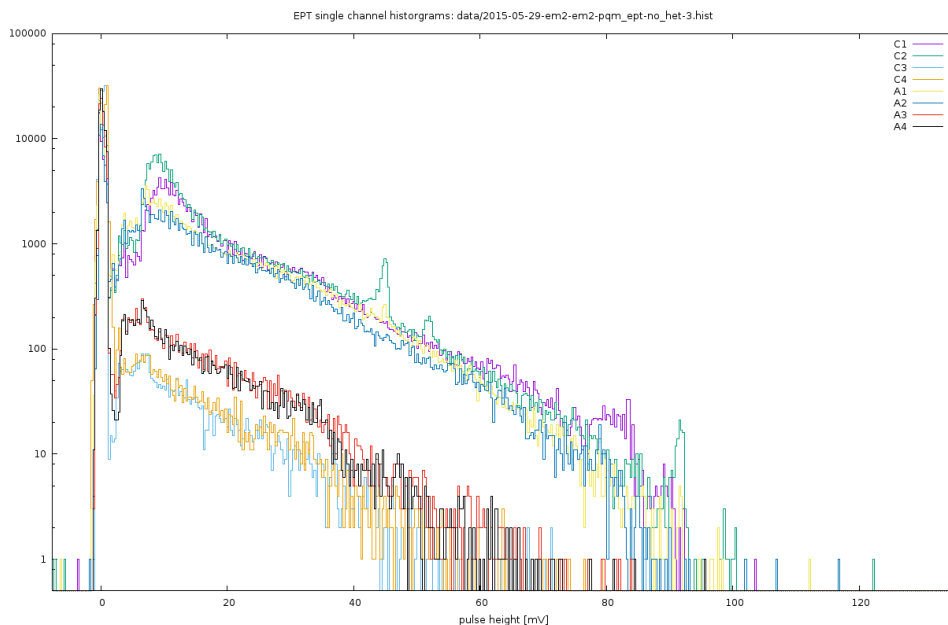
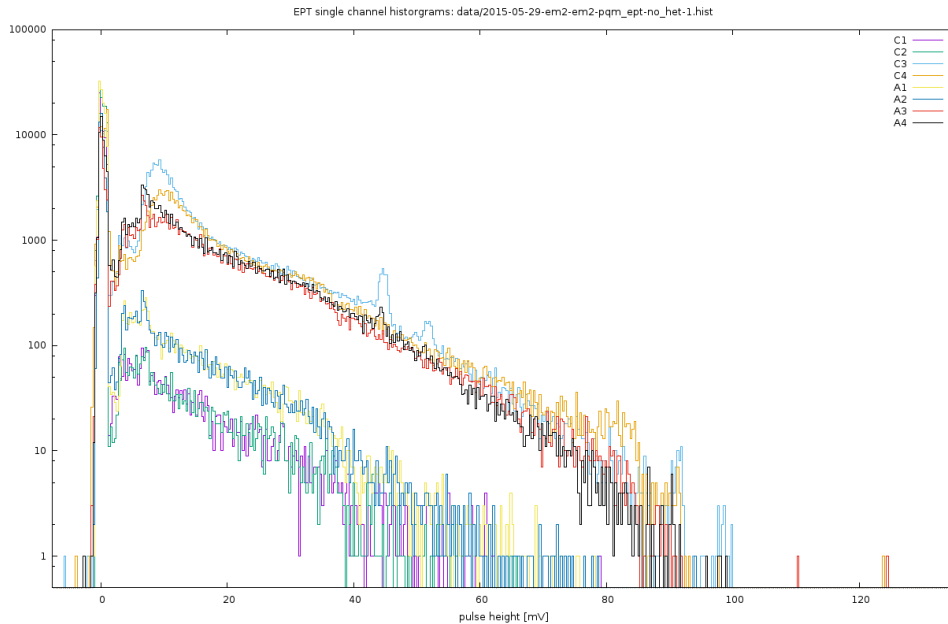
PQM EPT sensor head
EM2 Analog board
EM2 Digital board
LDO Power board
Bi207 source

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Telecom Alexander Hannes OHB

Analysis from photos of damage:

LVPS – staking was not adequate for the capacitors; the PWM generator was glued to the neighbouring capacitor due to close proximity, but had not been intended to be staked at all.

Digital and Analog board FPGAs – the issue is, the FPGA is not adequately supported by the mechanical frame; this is worst for the Analog board where the FPGA is in the center of the board.

Comments and suggestions:

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The staking is better on the PQM STEP LVPS.

Bending of the boards under vibration is the cause of the FPGA broken legs; stiffening the boards by using thicker pcb would help, and improving the fixation of the boards to the frame would help.

For testing STEP, notching during vibration would avoid the same problem with FPGAs.

Notes by M.L.Richards, 2015-06-03