- 5.5 Electrical interface
  - Please provide the instrument power budget analysis in each operation mode and state what margin level is used.

LGR_MEPS

MEPS A + MEPS B 36 ADCs

3 channels single gain and 3 channels dual gain for each MEPS Detector Package
Preamps = 6*2 + 6*2 = 24
Shapers = 9*2 + 9*2 = 36

MEPS detector package(2per sensor, 2 sensors per unit, 2units) 9 channels per package, 18 channels per sensor, 36 channels per unit.

QTY	DESCRIPTION	POWER / mW	POWER TOTAL / mW	misc Infos comments	Board
12	Preamps (1 BF862 FET @ 5V, 1 AD8005 +-5V Iq=0,4mA)	14.00	168	MEPS A preamps	MEPS A Filter & Preamp
12	LDO dissipation loss for BF862, power supply from +6V analog	4.00	48	it's just one LDO for FET	MEPS A Filter & Preamp
1	3x (LDO PREAMP POS + LDO PREAMP NEG + JFET) 4 OPs 4*2.2mA*6V=52.8mW (LDO quiescence power)	52.80	53	LDO quiescence power, 1OP is unused	MEPS A Filter & Preamp
12	LDO dissipation loss for AD8005 power supply from +-6V analog (0.4mA*(2*6V-2*5V))=0.8mW	0.80	10	just four LDOs for +V-PA and -V-PA	MEPS A Filter & Preamp
12	Preamps (1 BF862 FET @ 5V, 1 AD8005 +-5V Iq=0,4mA)	14.00	168	MEPS B preamps	MEPS B PREAMP + FILTER
12	LDO dissipation loss for BF862, power supply from +6V analog	4.00	48	it's just one LDO for FET	MEPS B PREAMP + FILTER
1	3x (LDO PREAMP POS + LDO PREAMP NEG + JFET) 4 OPs 4*2.2mA*6V=52.8mW (LDO quiescence power)	52.80	53	LDO quiescence power, 1OP is unused	MEPS B PREAMP + FILTER
12	LDO dissipation loss for AD8005 power supply from +-6V analog (0.4mA*(2*6V-2*5V))=0.8mW	0.80	10	just four LDOs for +V-PA and -V-PA	MEPS B PREAMP + FILTER
36	Shaper (1 AD8005 +-5V Iq=0,4mA)	4.00	144	HET + EPT shaper	ANALOG FPGA SHAPER ADC
38	12bit 8Channel ADC ADC128S102QML (1.5mA @ 3.3V)	4.95	188	30x ADC shaper 2x ADC housekeeping	ANALOG FPGA SHAPER ADC
1	RTAX2000S radiation hardened FPGA – ACTEL	270.00	270	ADC interface, level trigger	ANALOG FPGA SHAPER ADC
1	misc amplifiers, misc electronic, temperature sensors, LDOs	150.00	150	temperature, divider misc electronic	ANALOG FPGA SHAPER ADC
1	multiple reference voltages	35.00	35	with reference chip and resistor divider for multiple voltages	DIGITAL
36	LDO dissipation loss for AD8005 power supply from +-6V analog (0.4mA*(2*6V-2*5V))=0.8mW	0.80	29	just four LDOs for +V-SH, -V-SH, +V-PA and -V-PA	DIGITAL
1	2x (LDO SHAPER POS + LDO SHAPER NEG) 2 OPs 2*2.2mA*6V=26.4mW (LDO quiescence power)	26.40	26	LDO quiescence power for shapers	DIGITAL
1	RTAX2000S radiation hardened FPGA – ACTEL	440.00	440	processing softcore EDAC UART	DIGITAL
1	RAM 16Mbit (2M x 8), SRAM,with continuously write cycles	90.00	90	data and softcore program SRAM EDAC UART ADC interface	DIGITAL
1	oscillator (20mA @ 3.3V)	66.00	66	Main clock for FPGA	DIGITAL
2	UT54LVDM055LV 1 out TX, 1 in RX, 1 in 1HZ NOM & RED (27.5mA @ 3.3V)	90.75	182	1Tx, 1Rx, 1Hz-clock NOM & RED	DIGITAL
1	80% switching regulator 5059RH for FPGA core voltage 1.5V	177.50	178	switching regulator V-Digital	POWER
1	80% switching regulator 5059RH for IO voltage 3.3V	70.63	71	switching regulator V-Digital	POWER
1	80% switching regulator 5059RH for analog ADC voltage 3.3V	47.03	47	switching regulator V-ADC	POWER
1	PWM switching frequency synchronisation crystal oscillator and CD4024	132.00	132	synchronisation with LVPS	POWER
1	2x (LDO ANALOG POS + LDO ANALOG NEG) 2 OPs 2*2.2mA*6.7V=29.48mW (LDO quiescence power)	29.48	29	LDO quiescence power for analog voltage	DIGITAL
1	LDO dissipation loss for analog power supply from +-6.7V analog to +-6V	131.08	131	LDO dissipation loss for analog LDOs	
	POWER		2764	POWER total all above	
	LOW VOLTAGE POWER SUPPLY (electrical Efficiency: 70%, VIN: 28V, VOUT: 4.9V, 2x6.8V, 21V, 12V, 12V)		1185	power loss LVPS	POWER
			3949	**TOTAL (no heater)**	
			4739	**+ Margin 20%**	

estimation for activity of 100% at 25°C

Figure 1: MEPS instrument power consumption estimation

- Please provide your instrument local ground scheme.

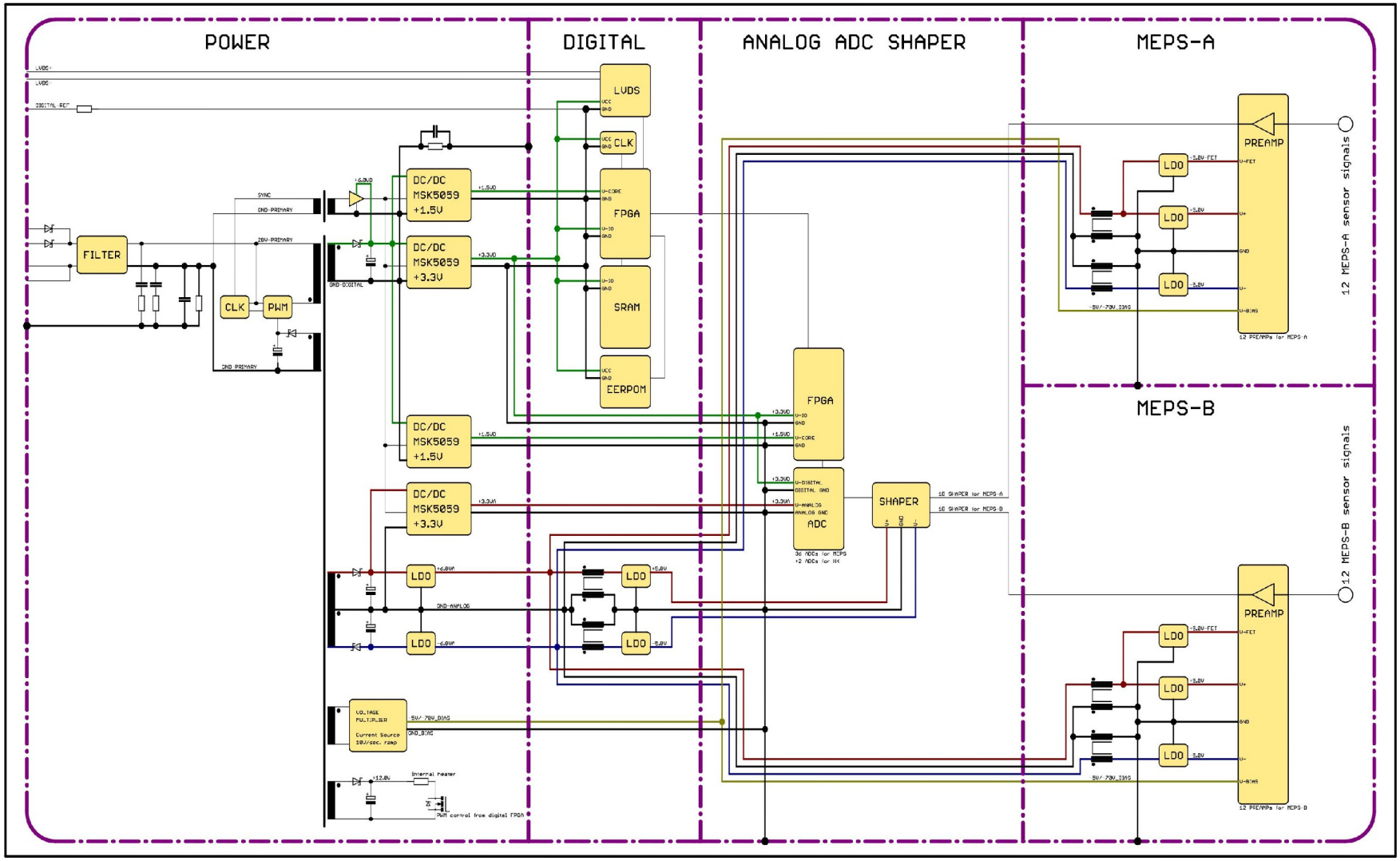

Figure 3: MEPS instrument ground schematic

- Please provide some information about the DC-DC converter you plan to use in your instrument, e.g. what secondaries are required? what efficiency you expect it to achieve at normal load? is this DC-DC transformer isolated(it should be)? Is it an off-the-shelf product or customized circuit?

- The voltage converter for the low voltage power supply (LVPS) is a flyback converter topology build with the Pulse width modulator(PWM).
- The clock frequency of the PWM generator is externally synced to 125kHz switching frequency(250kHz external sync). This frequency will be generated by a crystal oscillator with 2MHz. With this frequency divider the frequency of 1MHz for the secondary switching regulators (MSK5059) will be provided also. A common mode choke will be used as transformer to provide these switchers with external sync frequency.
- The PWM and the secondary switchers has adjusted frequency of around 75% of the desired and will be trimmed to the desired. So, when external sync to the wished fails, these regulators will run anyway.
- The flyback converter is regulated to a secondary output on the primary side, which will provide the PWM itself and the crystal oscillator with its frequency divider. So, no optocoupler is needed in this configuration.
- The outputs of the positive and negative analog voltages of the flyback converter has a down streamed LDO to minimize noise and provide a stable voltage for the further boards.
- The analog voltage for the ADCs(3.3V) will be provided by a switching regulator also, with an additional passive filter.
- The digital voltages will be provided by switching regulators (Vcore for FPGA 1.5V, VDigital IO 3.3V).
- There are two 12V output secondary voltages. One is the operating voltage of the PWM and clock along with the frequency divider and the second secondary12V is for the internal heaters if necessary.