The MSL RAD Second Level Trigger Algorithm

Stephan Böttcher

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This document describes the algorithms of the second level trigger module for MSL RAD EVIL.

1 The RAD three level trigger

The RAD instrument for the *Mars Science Laboratory* records the occurence of individual radioactive particles impinging on its detector systems. Several silicon detectors record an amount of electric charge deposited by the particle event, either directly into the silicon, or via scintillation light.

The frontend electronics amplifies the charge pulses into shaped voltage pulses. The back-end employs a VIRENA ASIC, an ADC, an FPGA called EVIL, and a digital electronics board with an embedded processor to further process the signals.

1.1 Level 1 trigger

The VIRENA ASIC implements the level 1 trigger. Any subset of the detector channels can be enabled for the level 1 trigger, each channel has a configurable discriminator threshold. When any enabled channel exceeds its discriminator threshold, a level 1 trigger occurs.

In response to a level 1 trigger, the VIRENA ASIC is put into hold mode, where all channel's pulse amplitudes are stored in analog peak-detector/hold circuits. Each detector channel in the VIRENA has an additional discriminator with a latch that records if a second threshold was exceeded by the pulse amplitude.

Both the peak-detectors and the second discriminators receive the input pulse after some additional shaping, to make sure that they properly register the peak voltage after a level 1 trigger occured.

The first set of discriminators is refered to as *fast* discriminators, and the second set as *slow* discriminators. The latched bits are refered to as *fast tokens* and *slow tokens*.

1.2 Level 2 trigger

The VIRENA ASIC is controlled by an FPGA called EVIL. The L2 trigger is implemented inside this FPGA. In response to a level 1 trigger, the EVIL will receive the latched bits from the second set of discriminators from the VIRENA, and based on these slow tokens a decision is made which detector channels shall be digitized for the event.

The level 2 trigger can be configured to trigger on up to 16 non-exclusive event classes. Each event class considers a configurable subset of the slow tokens, and requires this subset to match a configurable value. So each event class can be configured to define a set of coincidence and anticoincidence conditions, which must all be satisfied for that event class to trigger.

When an event class triggers, it requests a configurable subset of channels to be digitized. The union of the requested channels by all triggered event classes will be digitized.

The Level 2 module also does some processing of the digitized pulse amplitudes.

The Level 2 module does not actually reach a trigger decision whether to digitize or not. That dicision is made based on the status of the readout FIFO. The level 2 module aids that desicion by assigning each event class a high or low priority, and tell if any high-priority event class was triggered.

It is possible for an event to be digitized with zero channels being selected. The event data packet will only contain a header.

The level 2 module maintains a set of counters to count the occurens of fast tokens set, slow tokens set, triggered event classes, high and low priority events received and high and low priority events being digitized.

1.3 Level 3 trigger

For every event that is digitized an event data packet is sent to the embedded processor on the digital electronics board of the instrument. The level 3 trigger algorithm executed by the processor will classify the events based on the slow tokens, L2 event class, and digitized pulse amplitudes. This classification distinguishes particle types and energy. A set of histograms is accumulated. A subset of the events are recorded individually in compressed form for ground analysis.

The following sections describe the algorithms on the L2 module in detail.

2 L2 module Interfaces

The level two trigger module is written in Verilog HDL and incorporated in the EVIL FPGA design.

2.1 Output FIFO

All output[1] is sent via data packets though a FIFO interface. The L2 module produces three types of packes: type 0x00 are event data packets, type 0x01 are configuration readback packets, and type 0x02 are counter readout packets.

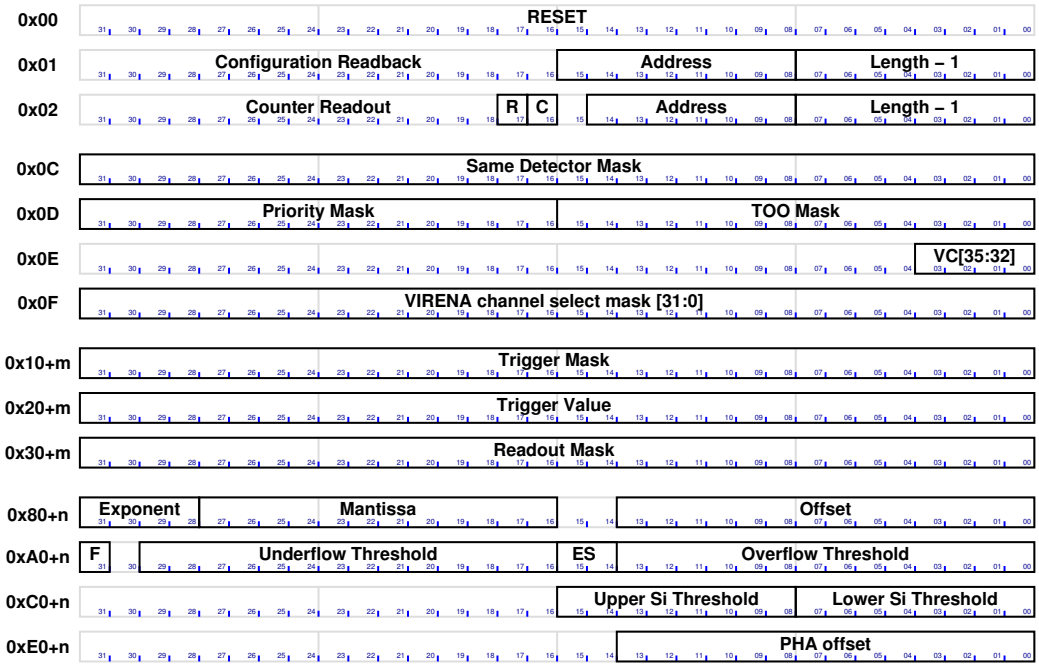

Figure 1: Configuration address space. The first three addresses are write-only commands. The index $m = [0..15]$ specifies the L2 event class, and the index $n = [0..31]$ is the detector channel.

2.2 Configuration registers

The L2 module is configured by writing 32-bit values into a 256 word configuration address space. Fig. 1 shows the format of all configuration registers.

[1]Except for the readout tokens.

These registers are refered to below by their hex address optionally followed by a bit range.

The contents of the configuration registers can be read back by sending a command to configuration address 0x01, specifying the address and number of words to read. The contents of the specified registers will be formatted into a packet and sent to the FIFO.

The second half of the configuration address space is occupied by a calibration memory block.

3 The level 2 trigger

3.1 VIRENA channel selection

The VIRENA has 36 analog channels. 36 is a cumbersome number. Two of those are test channels, and the remaining 34 channels are two redundant copies of each of the 17 front-end detector signals. The level 2 module operates on a subset of at most 32 channels. The remaining channels are completely ignored.

The configuration registers 0xE0 and 0xF0 specify which channels are selected. Each bit corresponds to the respective VIRENA channel number. Register 0xE0 selects VIRENA channels 32 to 35.

The selected VIRENA channels are mapped onto the 32-bit L2 numbering in the order the tokens arrive. The tokens come from the VIRENA starting with channel 35 going down to channel 0. The first selected channel becomes channel 0 in L2 numbering space. So the channel numbers reverse their order in L2.

3.2 Channels, detectors, and gains

Each physical detector element of the RAD instrument is processed by multiple channels. The scintillation detectors are read out by multiple silcion diodes with different sensitivity. The silicon detectors have multiple shapers in the front-end with different gain. Each front end signal is available on two VIRENA channels, which can be configured with different gains. In all cases, a higher gain channel shall have a higher VIRENA channel number than a lower-gain channel of the same detector.

The L2 module needs to know which channels belong to the same detector. There are two places where this needs to be configured.

The configuration register 0x0C *same detector mask* shall have a bit set for each channel which belong to the same detector as the previous channel,

in token order. I.e., only the highest gain channel of each detector has its bit reset. This register is used to make sure that any detector is always read out completely, even if the lower-gain channels did not trigger any discriminator.

The gain selection algorithm (see below) also needs to know which channels belong to the same detector. For that purpose there are separate configuration bits in the calibration memory.

3.3 Event classes

Event classes (index $m = 0..15$) are defined by a *trigger mask* (0x10+m), a trigger value (0x20+m), a readout mask (0x30+m), a priority bit (0x0D[$m+16$]), and a *TOO* bit (0x0D[m]).

3.3.1 Trigger

An event class triggers when all slow tokens selected by the trigger mask have the state specified in the respective trigger value bit.

When both the mask and value are all zero, the event class always triggers. When any value bit is 1 with the corresponding mask bit being 0, the event class is effectively disabled.

3.3.2 Readout

The *readout mask* configures which channels shall be digitized when the event class triggered. When the *TOO* bit is not set, the *readout mask* is used as specified, i.e., all channels selected in the *readout mask* are digitized.

When the *TOO* bit is set, only those channels are digitized which belong to a detector that has a slow token set. This assumes that the highest gain channel slow token is always set when any other slow token of that detector is set. Precisely, a channel will be digitized, when the corresponding *readout mask* bit is set, and the corresponding slow token was set or any higher gain channel of the same detector has the slow token set. The *same detector mask* specifies which channels belong to the same detector.

3.3.3 Priority

The *priority* bit configures the event class as high priority when set. When any triggered event class is high priority, the whole event is high priority. High priority events have a separate set of total event counters. The FIFO controller accepts low priority events events only when a significant fraction of the FIFO is empty, while high priority events are digitized unless the FIFO if almost full.

The level 3 trigger assigns a separate PHA priority to each event, which must not be confused with the L2 priority described here.

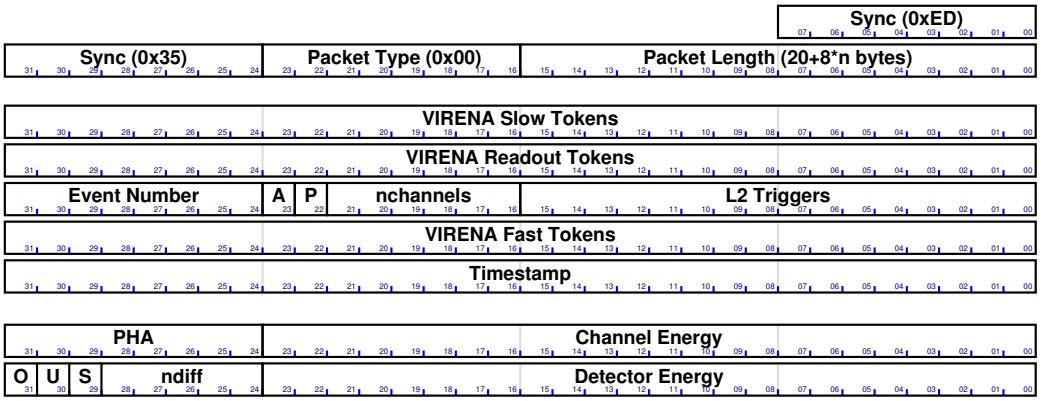

Figure 2: Event packet format. The EVIL packet header is five bytes long, including sync bytes, packet type, and packet payload length. The event data header is 5 words long, with 4 bytes per word. The event packet header is followed by two words (eight bytes) for each digitized channel.

4 ADC Data processing

When an event is selected for digitization by the FIFO controller, the combined readout mask of all event classes is transfered to the VIRENA to controll the analog multiplexer, and the selected channels are digitized.

4.1 Event packet header

While the readout tokens are transfered to the VIRENA, an event packet header is formatted and sent to the FIFO. The packet header consists of the EVIL packet header in the format common for all packets going from the EVIL to the digital board, and the event data header.

Fig. 2 shows the format of the event data packet. Event data packets are EVIL packet of type 0x00. The payload length is 20 bytes plus 8 bytes per digitized channel.

The event header is five words long, four bytes per word. The slow tokens are sent in the first word.

The second word is the combined readout mask. This word is essentially required to tell which channels correspond to the event data in the remainder of the packet.

The third word contains several bit fields. The first byte is an event number provided to the L2 module by the VIRENA controller module of the EVIL. Bit 23 is an attention bit where the EVIL can flag something to the digital board. Bit 22 is the event L2 priority. Bits [21:16] are the number of digitized channels. Bits [15:0] are the event classes that were triggered by this event.

The fouth word are the VIRENA fast tokens. The fifth word is a timestamp provided by the EVIL.

4.2 Channel data

The order of digitization is the opposite as the token order, i.e., the lowest numbered selected VIRENA channel is digitized first. After each digitization, the resulting ADC data word is transfered to the L2 module for processing. The L2 module receives the channels of each detector ordered from low gain to high gain.

The data processing is configured by a 128 words configuration memory, with 32 bits per word. Each channel is independently configured by four words.

Each digitized channel produces two words (eight bytes) of output in the event data packet, which follow the data packet header.

Fig. 3 shows a block diagram of the data processing.

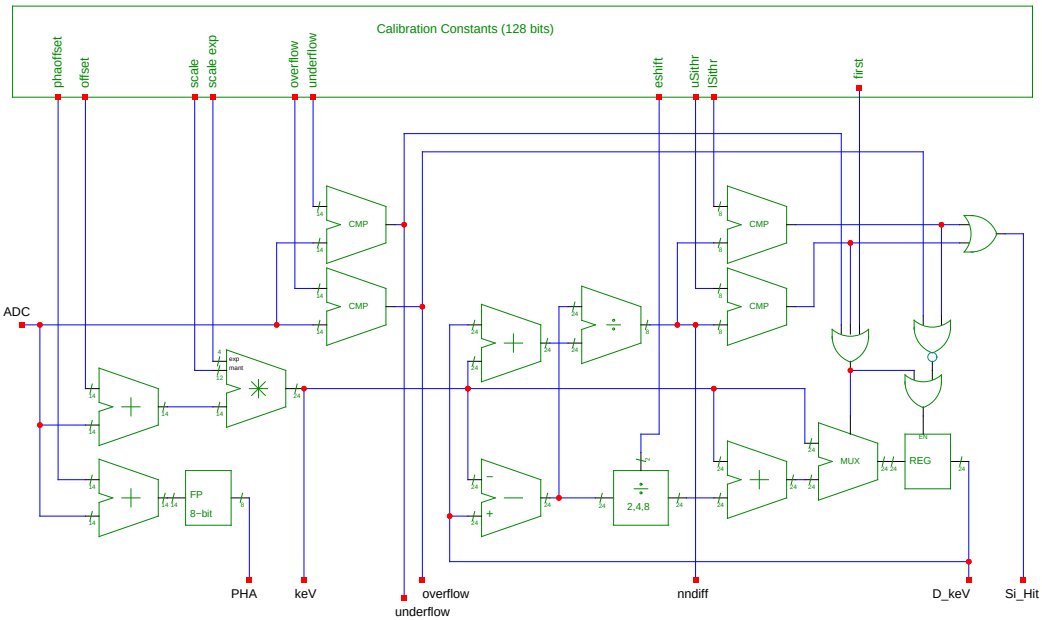

Figure 3: Level two data processing.

4.2.1 Calibration

The ADC delivers the pulse height as a 14-bit unsigned number, with some pedestal that varies from channel to channel, and a scale that depends on the detector sensitivity, preamp sensitivity, shaper gain, and the configurable VIRENA input gain.

For level three processing, the ADC result is converted to a 24-bit unsigned number with zero pedestal and a common energy scale for all detectors. A 14-bit signed offset p is added to the ADC result D, with overflow/underflow clipping. The offset is usually negative. The pedestal corrected value is multiplied by a 12-bit unsigned mantissa m, and then shifted right by a 4-bit unsigned exponent e.

$$E = \mathrm{floor}((D + p) \cdot m \cdot 2^{-2-e} + \frac{1}{2}) \tag{1}$$

The result E is sent to the FIFO in bits [23:0] of the first channel data word.

4.2.2 PHA data

The level 3 trigger will select a subset of events for analysis on the ground. For that purpose, the ADC results of each channel shall be converted to an 8-bit floating point number to fit more events into the telemetry allocation.

Since the ADC results come with a substantial pedestal, a PHA offset p' is added to the ADC result before conversion. The PHA offset shall be negative, but smaller in magnitude that the calibration offset, so that the distribution of values around the pedestal can be studied.

The floating point value is unsigned, 3-bit exponent e, 5-bit normalized mantissa m with implicit leading 1. An exponent value of zero means a non-normalized mantissa. To recover an approximation of the original ADC result, use:

$$D = \begin{cases} 4m - p' & \text{for} \quad e = 0 \\ (m + 32) \cdot 2^{e+1} - p' & \text{for} \quad e > 1 \end{cases} \tag{2}$$

The floating point representation is sent in the first byte of the channel data record.

4.3 Gain selection

The level 2 module attempts to estimate the energy deposited in a given detector based on the ADC results of all its channels. Each channel is processed in turn, starting with the lowest gain. The result is a current best estimate of the detector energy, called E_{sum}. This value is sent to the FIFO in bits

[23:0] of the second word of the channel data record. E_{sum} is also carried over for the next channel processing. The last, highest gain channel's E_{sum} can be used by level 3 as the overall result for the detector.

The lowest gain channel shall be marked by the *First* bit in the calibration memory, register bit (0xA0+n)[31]. When this bit is set, the calibrated energy is copied to the E_{sum}, and no further conditions considered.

Otherwise, the ADC result is compared to the *overflow threshold* (0xA0+n)[13:0]. When the ADC result exceeds that threshold, the channel result is ignored, and the previous E_{sum} value is kept. The threshold shall be configured so that values below are in the linear response range of the channel. Values beyond overflow threshold are discared in preference of the results of lower gain channels. An overflow is flagged in bit [31] of the second channel data word.

Otherwise, the ADC result is compared to the *underflow threshold* (0xA0+n)[29:16]. When the ADC result is below the underflow threshold, the previous E_{sum} is ignored, and the calibrated energy from this channel is copied to E_{sum}. The underflow threshold shall be configured so that ADC values below indicate that the previous, lower gain channels cannot usefully contribute anything but noise to the result. An underflow is flagged in bit [30] of the second channel data word.

4.3.1 Si-hit detection

When the channel is not first, not in overflow nor in underflow, then a silicon hit detection is attempted. The scintillation detectors are read out with multiple photo diodes. When a particle deposits energy in the scintillator, all diodes should see about the same charge, and the calibrated energy of all channels should match. When a particle hits the pin diode itself, that channel will show a much large signal compared to the others. The larger value shall be discared.

The L2 module computes a normalised difference of the calibrated energy E and the previous E_{sum}:

$$N = 64 \cdot \frac{E_{\text{sum}} - E}{E_{\text{sum}} + E} \tag{3}$$

The result N is compared to an upper or lower *silicon hit threshold* depending on the sign of N.

The five most significat bits of N are sent to the FIFO in bits [28:24] of the second channel data word.

If N is positive, and exceeds the *upper silicon hit threshold* (0xC0+n)[15:8], then the previous E_{sum} is much larger than what this channel says is should

be. In this case the previous E_{sum} is ignored, and the current channel calibrated energy is copied to E_{sum}. A silicon hit is flagged in bit [29] of the second channel data word.

If N is negative and below the *lower silicon hit threshold* (0xC0+n)[7:0], this channel has a much larger energy signal than the previous channels. The new result is discared and the old value for E_{sum} is kept. A silicon hit is flagged in bit [29] of the second channel data word.

4.3.2 Linear combination of energy readings

When none of the above conditions are satisfied, we assume that the previous E_{sum} may contribute signal above noise and this channel even more, since it is higher gain. The new E'_{sum} is computed as a linear combination of the previous E_{sum} and this channels calibrated energy E:

$$E'_{\text{sum}} = E + k \cdot (E_{\text{sum}} - E) \tag{4}$$

where k can be be configured to be 0, 1/2, 1/4, or 1/8. The selection is done via the ES bits in (0xA0+n)[15:14]:

ES	k	Formula
0	0	$E'_{\text{sum}} = E$
1	$\frac{1}{2}$	$E'_{\text{sum}} = \frac{1}{2}E + \frac{1}{2}E_{\text{sum}}$
2	$\frac{1}{4}$	$E'_{\text{sum}} = \frac{3}{4}E + \frac{1}{4}E_{\text{sum}}$
3	$\frac{1}{8}$	$E'_{\text{sum}} = \frac{7}{8}E + \frac{1}{8}E_{\text{sum}}$

5 Counters

The L2 modules maintains a memory block full of counters. Each counter is 32 bits wide. The memory block has space for 128 counters.

There are two phases when counting happens: Phase 1 is when the VIRENA tokens come in, i.e., all L1 triggered events. Phase 2 is when the readout tokens go out, i.e., an event is being digitized.

5.1 Phase 1 counters

When the slow and fast tokens are serially received from the VIRENA in responce to a L1 trigger, each token is counted. There are 32 counters for the slow tokens and 32 counters for the fast tokens.[2]

[2]The fast tokens can be counted only when the token shifting does not proceed at full clock speed.

When all tokens were received, a total event counter is incremented. There are two total event counters, one for high priority events, one for low priority events.

Afterwards, a counter for each triggered event class is incremented.

5.2 Phase 2 counters

When the FIFO controller decided to digitize the event and commands the L2 module to shift out the readout tokens, another set of total event counters and event class counters is incremented. This allows to scale the count rates in the L3 histograms by the fraction of L1 events that could be digitized.

The counter addresses are:

number	phase	counter
(0x00+n)	1	VIRENA fast token counters
(0x20+n)	1	VIRENA slow token counters
(0x40+m)	1	L2 event class counters
(0x50+m)	2	L2 event class counters, digitized
0x60	1	low priority total events counter
0x61	1	high priority total events counter
0x62	2	low priority total events counter, digitized
0x63	2	high priority total events counter, digitized

5.3 Counter readout

The counters are read by sending a command to configuration address 0x02. The specified counters are formatted into a counter readout packet and sent to the FIFO.

The counter readout command has two option bits: When bit [16] is set, the specified counters will be cleared. When bit [17] is set, no data is sent to the FIFO, to allow clearing of counters without readout.