MSL RAD EVIL
L2 trigger FPGA code review

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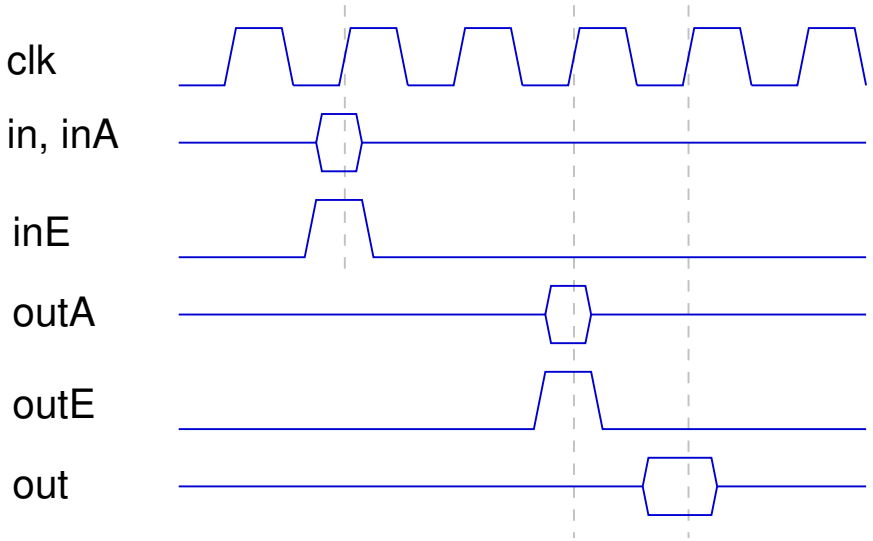
- 100 % synchronous.
- Single clock (24 MHz).
- Semi-structural coding style.
- Every sequential cell is explicit in the code.
- Runs without reset, i.e., all non-nominal state flushes out while processing an event.

```
wire a = ...;
reg b;
always @(posedge clk)
  if (...)
    b <= ...;
  else if (...)
    b <= ...;
  else
    b <= ...;
```

- The L2 trigger configuration is stored in cells.
- Calibration and Si-hit configuration is stored in SRAM.
- Event and trigger counters are stored in SRAM.
- Two instances of **module** sram128x32(); 128 words of 32 bits.



- Revision controlled since December 2005.
- CVS, *Concurrent Versions System*.

```
// $ Id: l2trig.v,v 1.32 2007/07/22 20:29:26 bottcher Exp $
//
// $ Log: l2trig.v,v $
// Revision 1.32  2007/07/22 20:29:26  bottcher
// minor documentation typo fix
//
// Revision 1.31  2007/07/22 18:21:45  bottcher
// rounding implemented in float8
//
// Revision 1.30  2007/07/22 12:36:09  bottcher
// fix bug in esuma: signed diff
//
// Revision 1.29  2007/07/19 22:43:59  bottcher
// phaoffset feature added
```

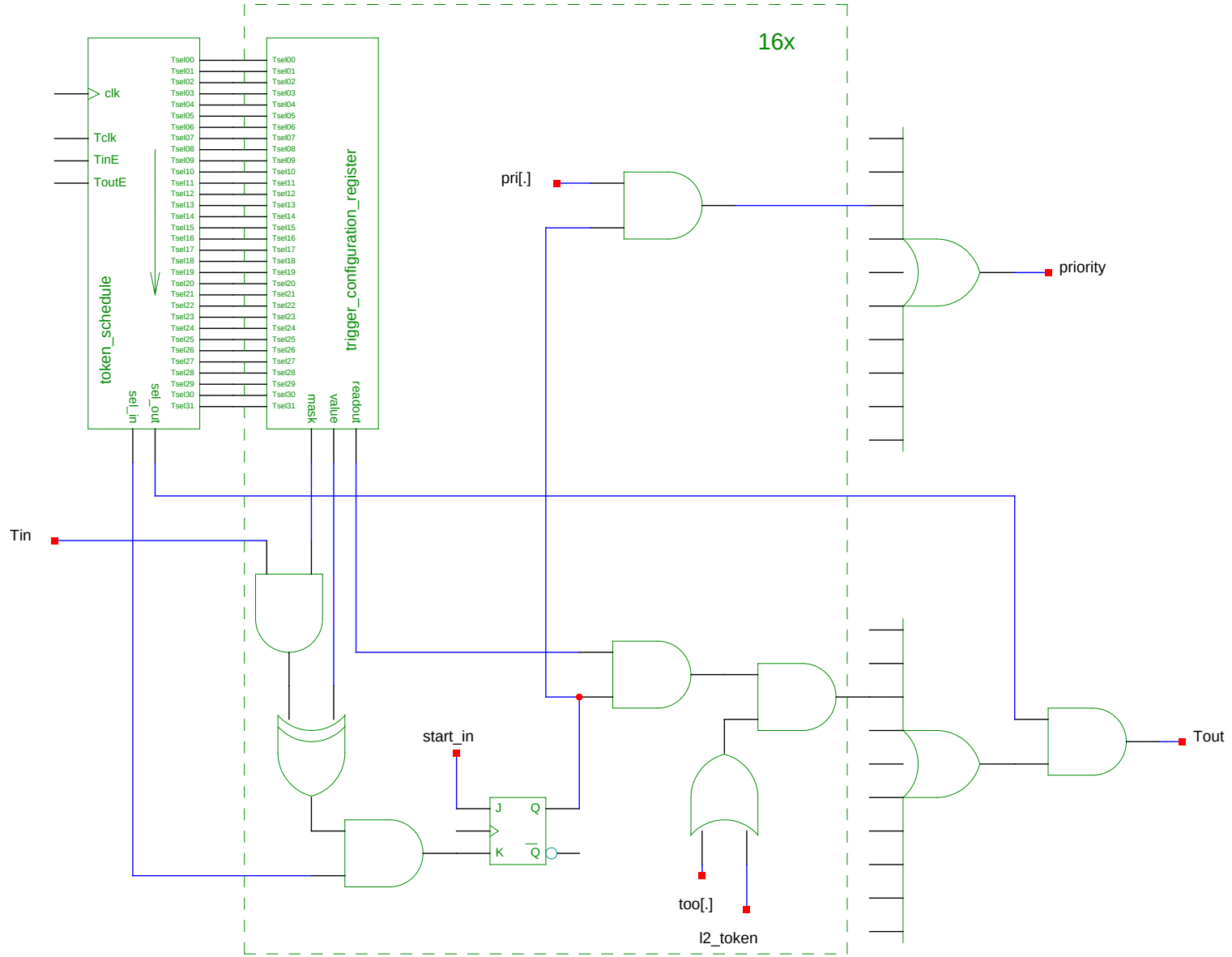
- Simulator: Icarus Verilog 0.8.5.
- Waveform viewer: GTKWave v3.0.30.
- Verilog testjig with:
  - Driver logic and tasks for all input interfaces.
  - Driver logic and monitors for all output interfaces.
  - All I/O is logged to a (text) logfile.
- The logfile is compared to a (revision controlled) gold file after each run.
- After changes to the l2trig module, the diff between logfile and goldfile highlights the changed behavior, aiding verification of the change.

```
module l2trig
  (clk,                 // 24 MHz clock
   reset,               // synchronous reset
   Tclk,                // Token clock phase

   Tin, TinE,           // L1 token serial input and enable
   Tout, ToutE,         // ADC token serial output and enable

   priority,            // priority trigger detected
   nchannels,           // number of channles to digitize

   data,                // ADC data comes in here
   dataE,               //  when strobed here.

   Fout, FoutE,         // FIFO output and enable
   FoutBusy,            // Unfinished packet

   Cini,                // Configuration input
   CinAi, CinEi         // Configuration address, enable
   );
```

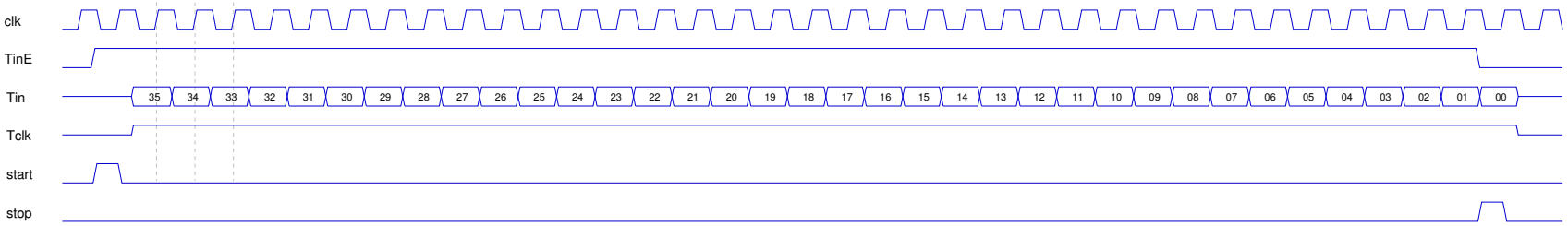
```
wire    Reset = reset | CinE & (CinA == 0);
```

- The reset is affecting registers that do not come out clean from unknown state during simulation, or that may cause spurious output before they settle down in a quiescent state.
- No reset is required to recover the l2trig module from arbitrarily corrupted states.
- The reset puts the l2trig module immediately into nominal idle state.

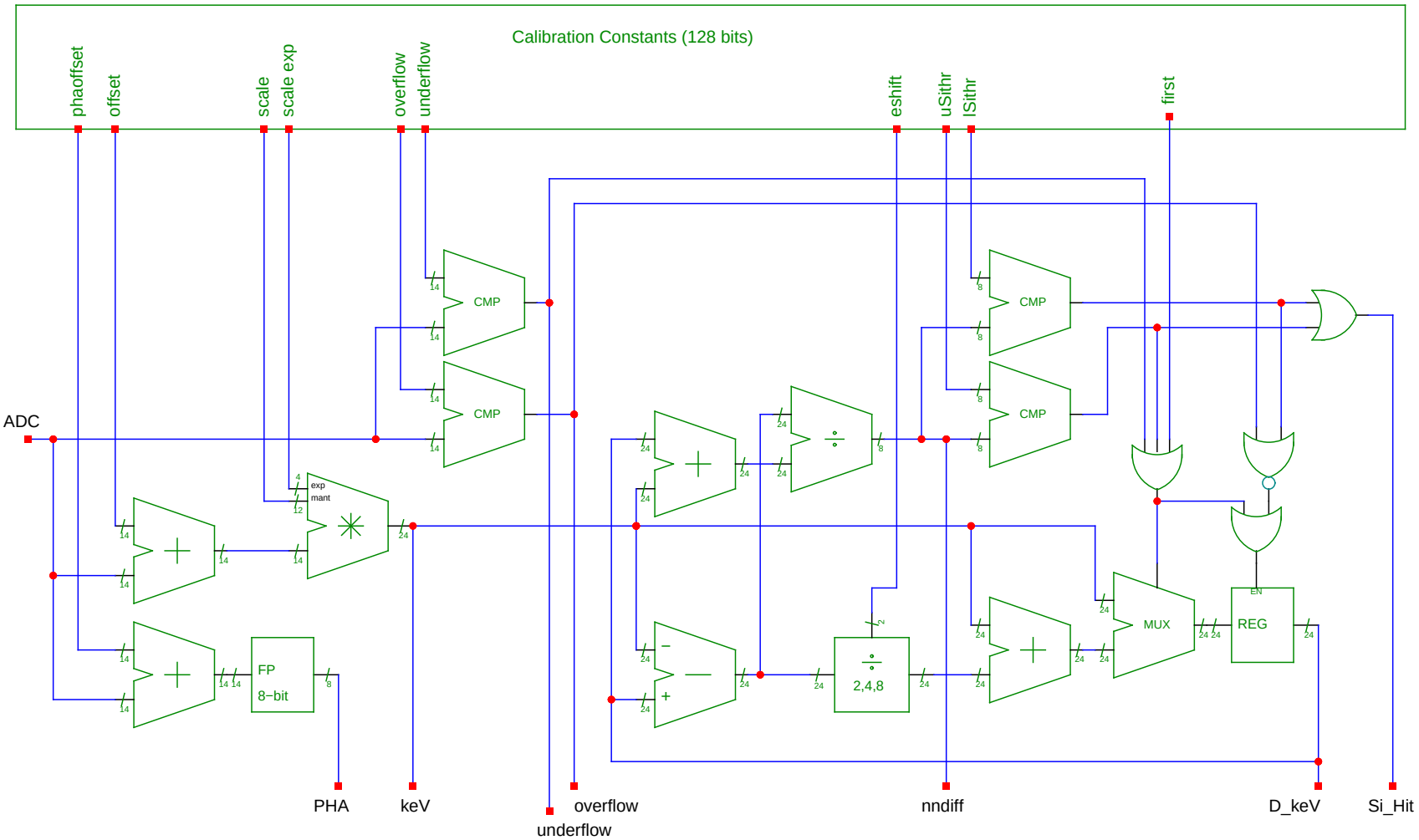
- Tin phase
  - ⇐ Serially receive VIRENA slow tokens.
  - ⇒ Count each slow token.
  - ⇒ Evaluate trigger conditions, priority.
  - ⇒ Count event (priority).
  - ⇒ Count matched triggers.
- Tout phase
  - ⇒ Serially send VIRENA readout tokens.
  - ⇒ Send event packet header to FIFO.
  - ⇒ Count event (priority).
  - ⇒ Count matched triggers.
  - ⇒ Fetch first set of calibration constants.
- Digitization phase
  - ⇐ Receive 14-bit ADC result.
  - ⇒ Calculate the energy.
  - ⇒ Convert ADC value to floating point.
  - ⇒ Perform gain selection.
  - ⇒ Send channel data to FIFO.
  - ⇒ Fetch next set of calibration constants.


16x
clk
Tclk
TinE
ToutE
token_schedule
sel_in
sel_out
trigger_configuration_register
mask
value
readout
Tsel00
Tsel01
Tsel02
Tsel03
Tsel04
Tsel05
Tsel06
Tsel07
Tsel08
Tsel09
Tsel10
Tsel11
Tsel12
Tsel13
Tsel14
Tsel15
Tsel16
Tsel17
Tsel18
Tsel19
Tsel20
Tsel21
Tsel22
Tsel23
Tsel24
Tsel25
Tsel26
Tsel27
Tsel28
Tsel29
Tsel30
Tsel31
pri[.]
priority
Tin
start_in
J
Q
K
Q
Tout
too[.]
l2_token

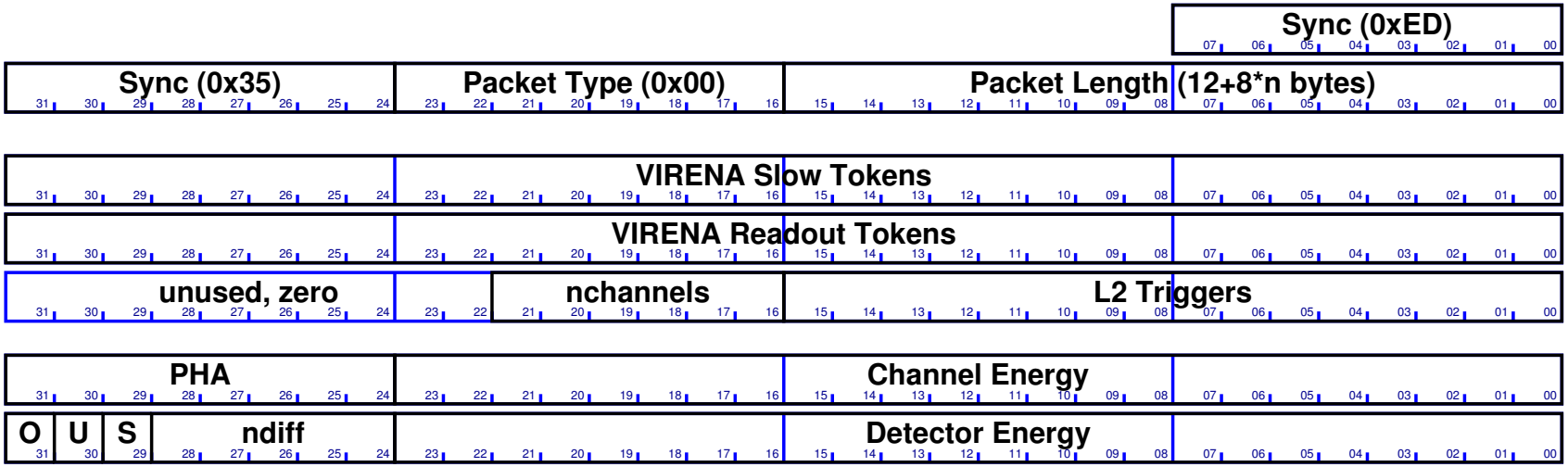
L2 trigger



- VIRENA channels are numbered 0 to 35.
- Channels 0 and 35 are unused edge-channels.
- Channels 1 to 34 are connected to 17 RSH outputs.
- Every RSH output is connected to two adjacent VIRENA channels.
- Multiple RSH channels belonging to the same detector are connected with the higher gains at higher numbered channels.
- The VIRENA tokens are serially shifted highest number first, i.e., 35 downto 0.
- The L2 trigger relies on getting high-gain first, to selectively read out channels from triggered detectors.
- For digitization, the VIRENA multiplexer delivers the output voltage of the lowest numbered channel first.
- The gain selection relies on seeing the low-gain channels of each detector first.



Verilog modules calibrate () and gainselect ().



- Five byte EVIL packet header, type 0.
- Twelve byte event header.
- Eight bytes per readout channel.

The number of read channels appears three times:

1. Packet length.
2. Explicit number in the event header.
3. Number of bits set in the VIRENA readout tokens.