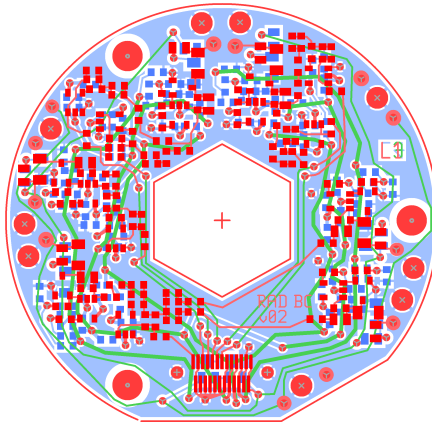


# MSL RAD Front-End-Electronics RADBC PCB layout

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The RADBC board supports the readout of the lower two *Solid State Detectors* (SSD) of the RAD instrument.

The board will be mounted in close proximity to the detectors, with the backside facing the detector, via three mounting holes.

The particle telescope field of view runs through a hole in the center of the board. The board's outer shape is circular with a diameter of 57 mm, and the central hole is hexagonal with a flat to flat width of 18 mm.

The detector is connected via Teflon insulated wires (AWG 32). These wires will be routed through holes in the RADBC board and soldered to pads on the front side. The RADBC board connects to a flex strip via an Omnetics Dualobe connector, 25-pin, vertical surface mount receptacle.

The electronics on the RADBC board include six *Charge Sensitive Amplifiers* (CSA), six *Fast Shapers* (FSH), and a separate detector bias filter for the detector guard rings.

# 1 Fabrication

The board shall be made according to IPC 6012 class 3 standards.

## 1.1 Material

The base material is polyimide glass, Total board thickness  $1\text{ mm} \pm 10\%$ , with  $35\text{ }\mu\text{m}$  copper thickness, surface finish HAL PbSn, with solder masks on both sides, *no* silk screens.

## 1.2 Design Rules

The minimum trace width is 0.2 mm (8 mil), clearance 0.2 mm (8 mil), the clearance on top surfaces to copper carrying  $-70\text{ V}$  shall be 0.3 mm (12 mil).

The minimum via hole diameter is 0.4 mm (16 mil), with annular rings of at least 0.25 mm (10 mil) width.

The edge clearance of copper traces and pads is 0.5 mm (20 mil) minimum.

## 1.3 Layers

The board has four copper layers, with SMD components on both sides. All components which carry AC signal are located on the top side. The backside is filled with a ground plane.

The inner layers are a ground plane and a power routing layer. The layer order is front, ground, power, back. The ground plane has cutouts under the inverting input nodes of the current feedback amplifiers (AD 8005).

Layer order	Gerber file
1 front layer copper	v02.group0.gbr
2 ground layer copper	v02.group3.gbr
3 power layer copper	v02.group4.gbr
4 back layer copper	v02.group1.gbr
board shape	v02.group2.gbr
1 front solder mask	v02.frontmask.gbr
4 back solder mask	v02.backmask.gbr
drill file	v02.plated-drill.cnc
1 front solder paste	(v02.frontpaste.gbr)
4 back solder paste	(v02.backpaste.gbr)
1 front silk screen	(v02.frontsilk.gbr)
4 back silk screen	(v02.backsilk.gbr)
fab, please ignore	(v02.fab.gbr)

The files in parenthesis are PCB tool output not relevant to this board's fabrication.

## 1.4 Outline

The central hexagonal cutout shall be made with a corner radius not larger than 1 mm.

## 2 Design

### 2.1 Tools

The design is done with GNU EDA tools. (<http://www.geda.seul.org/>)  
The layout tool is PCB version 20060822. GAF version is 20060824.

### 2.2 Schematics

The schematics for the CSA and FSH were derived from master schematics (Fig. 2 and 3) by a script which prefixes net names and reference designators with an instance prefix, L1\_ and L2\_ for the CSAs, and S1L\_, S1H\_, S2L\_, and S2H\_ for the shapers. The RADBC schematics (Fig. 1) defines connections between the amplifier instances and to the connector, as well as the bias filter and the thermistor.

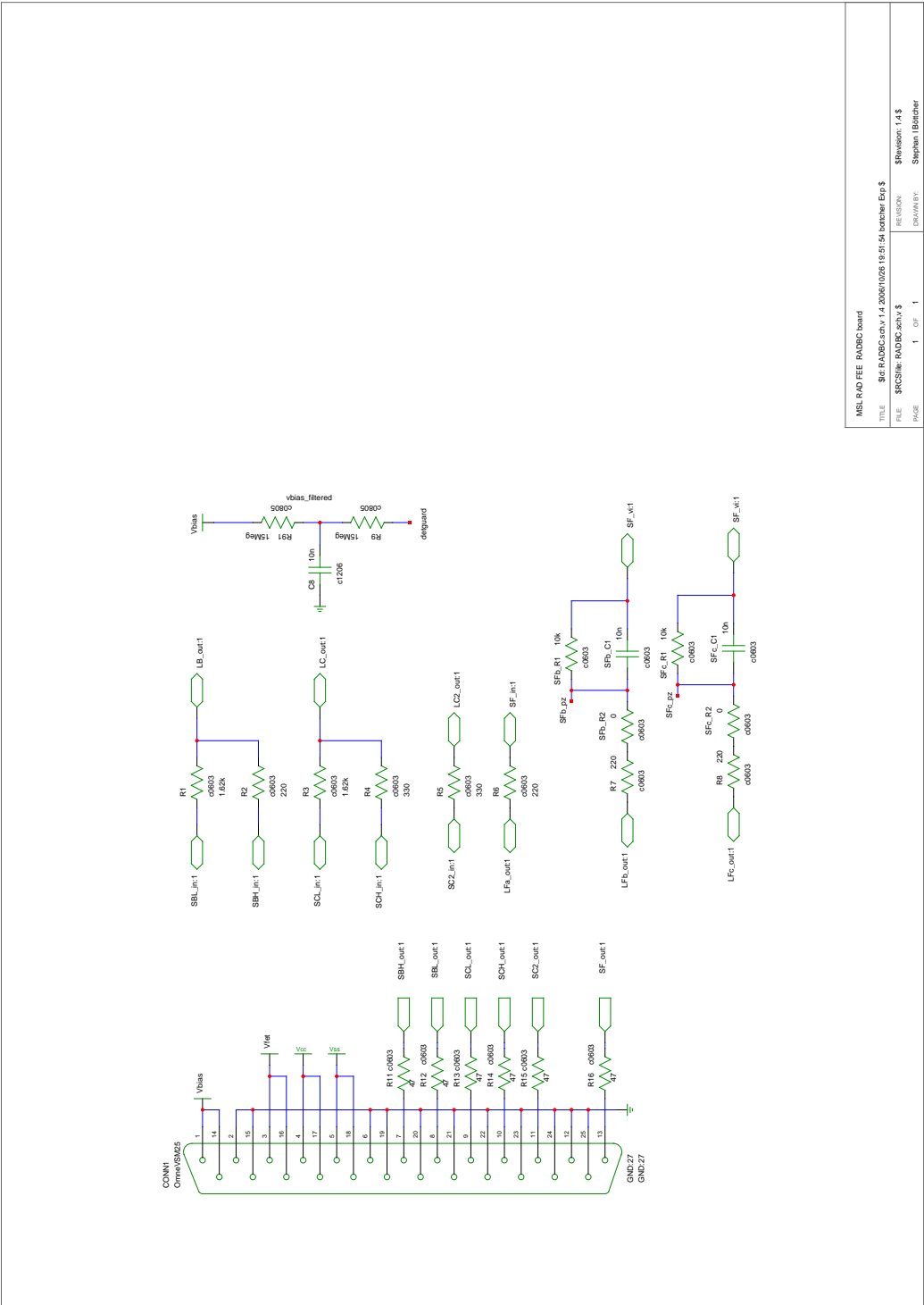
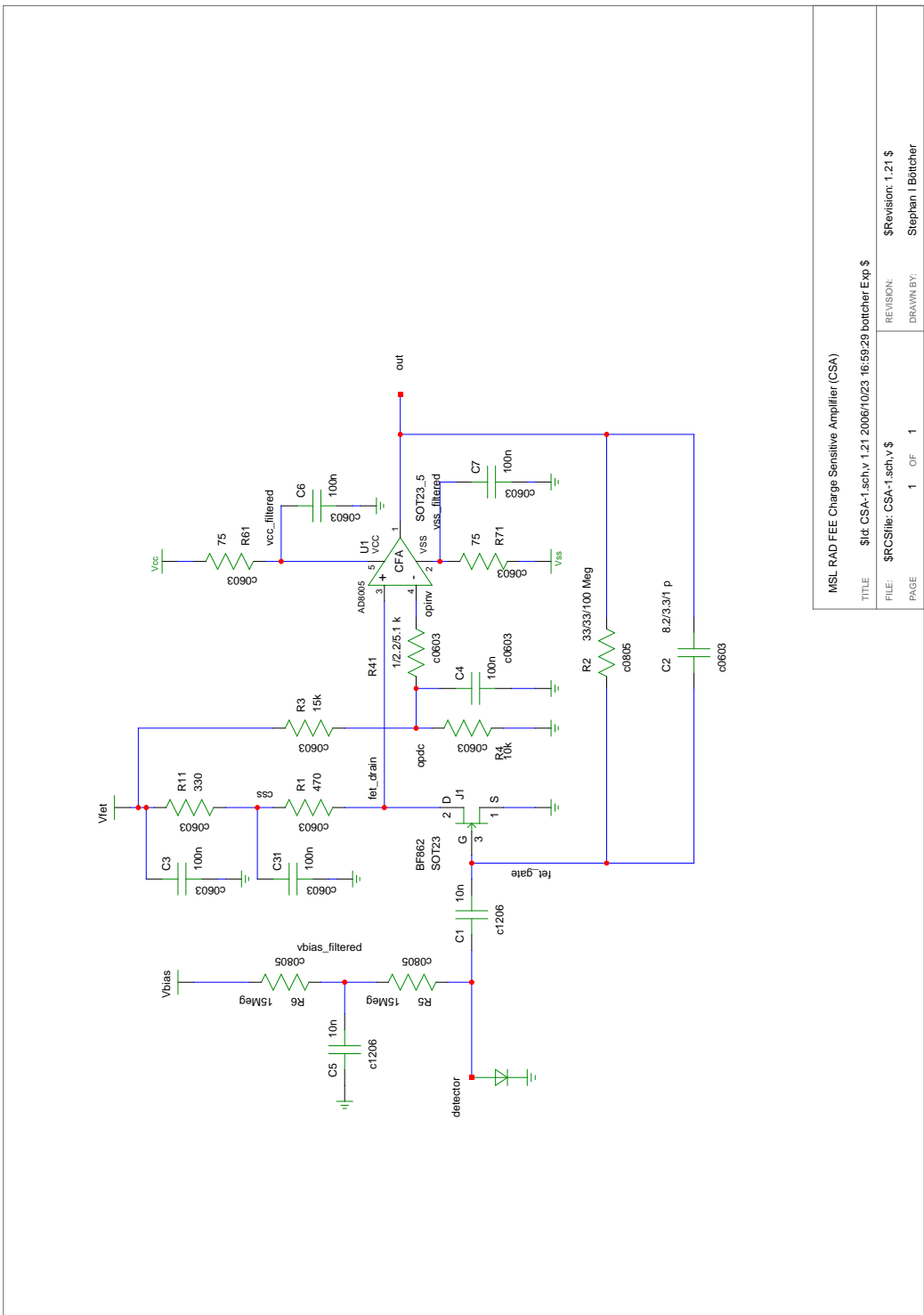


Figure 1: RADBC master schematics: RADBC.sch



MSL RAD FEE Charge Sensitive Amplifier (CSA)

TITLE: \$Id: CSA-1.sch,v 1.21 2006/10/23 16:59:29 bortcher Exp \$

FILE: \$RCSfile: CSA-1.sch,v \$

REVISION: \$Revision: 1.21 \$

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Figure 2: Charge sensitive amplifier schematics: CSA-1.sch

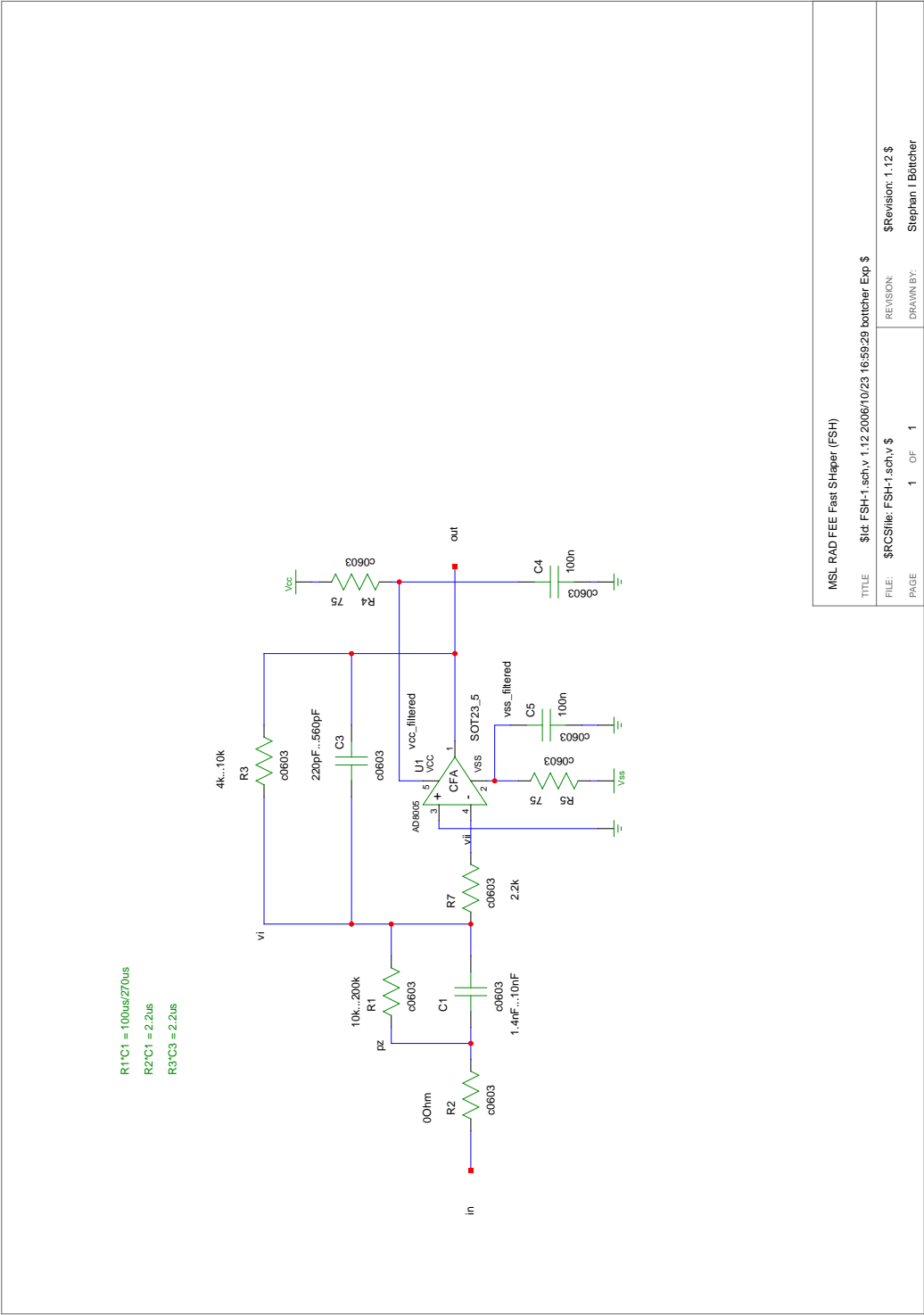


Figure 3: Fast shaper schematics: FSH-1.sch

## 2.3 Layout

Fig. 4 to 7 show the copper layer layouts, Fig. 8 and Fig., 9 show front and back pads with silk screen layers.

Each layer is shown at scale 1:1 and expanded to text width.

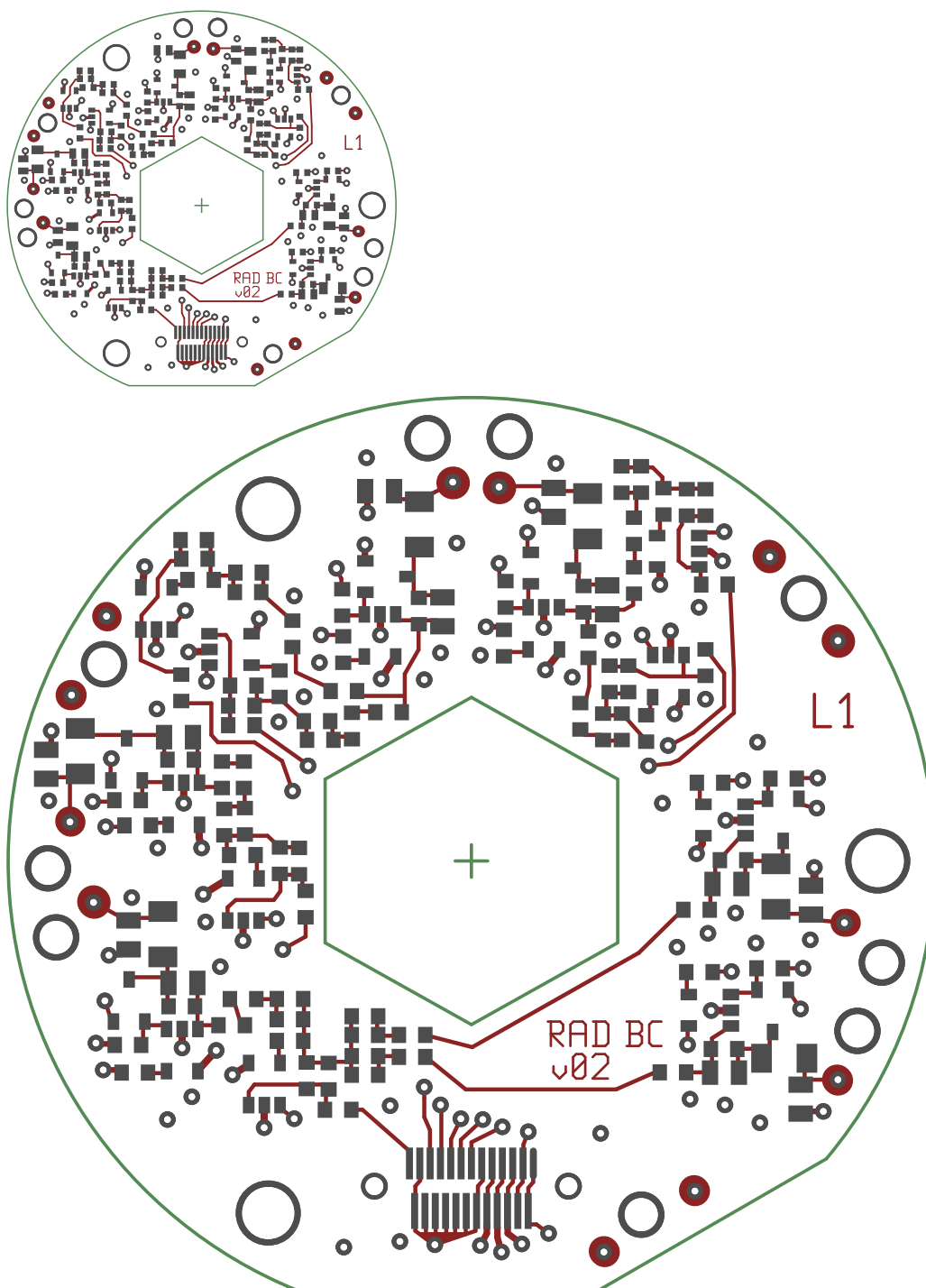


Figure 4: Front layer copper



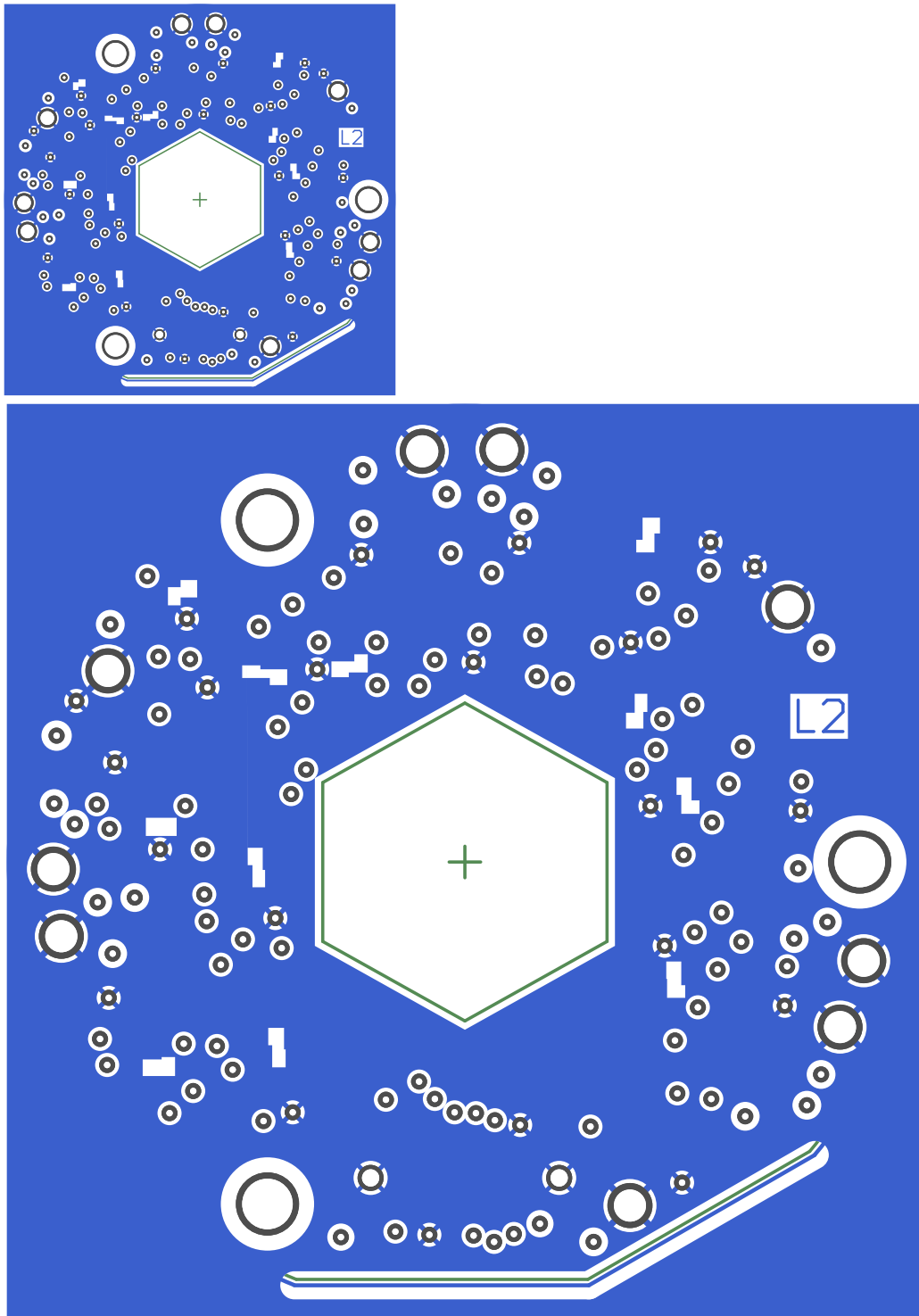


Figure 5: Ground layer copper

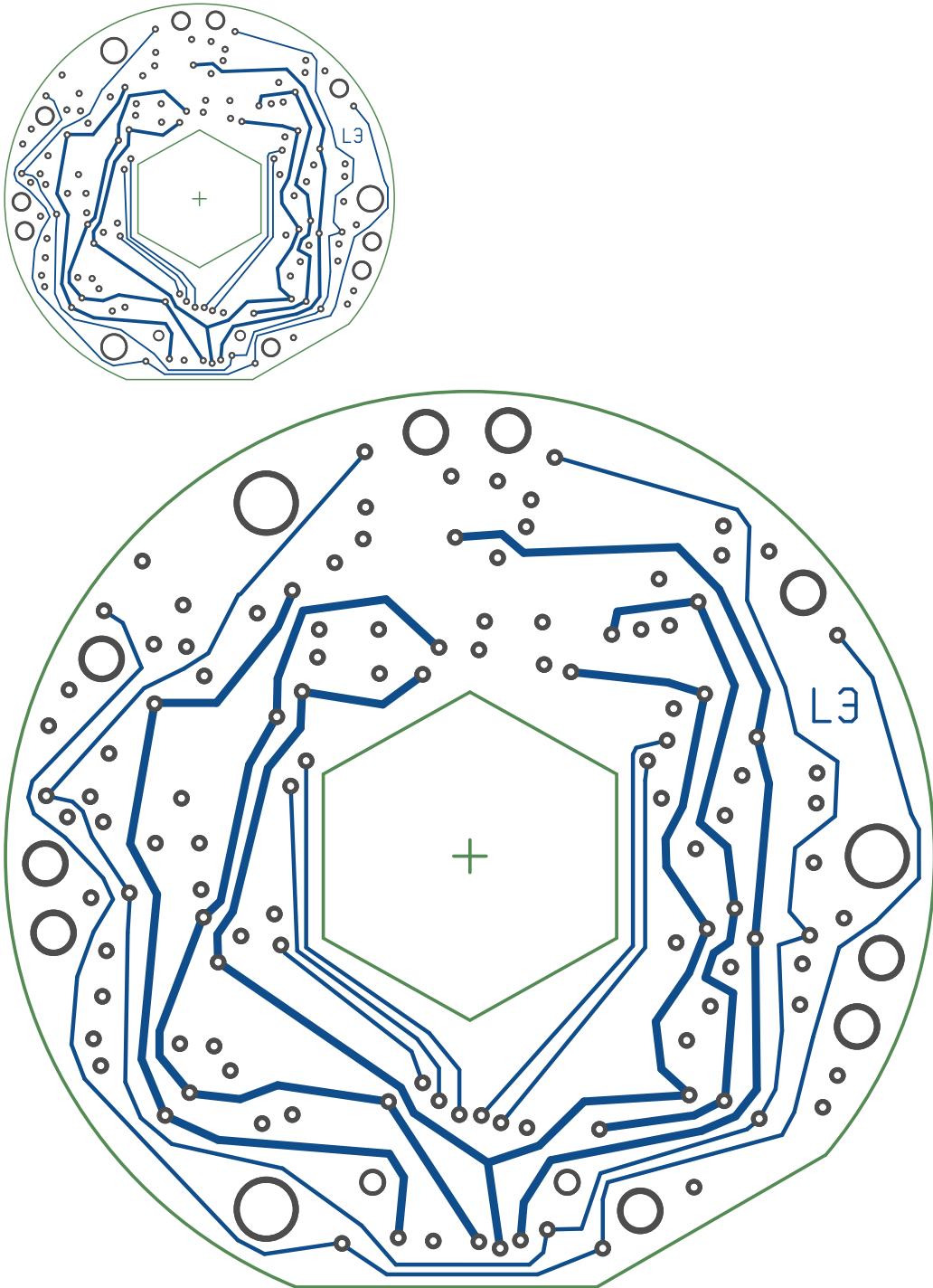


Figure 6: Power layer copper

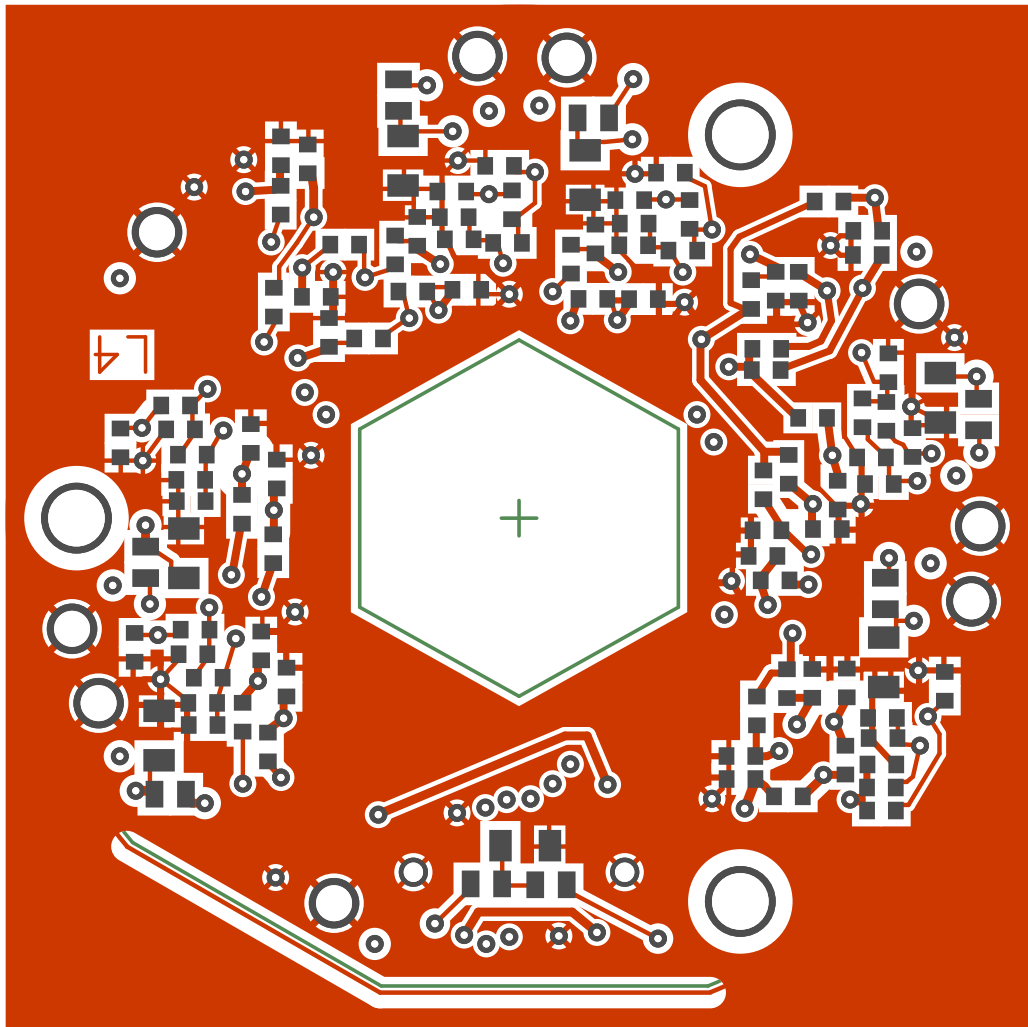
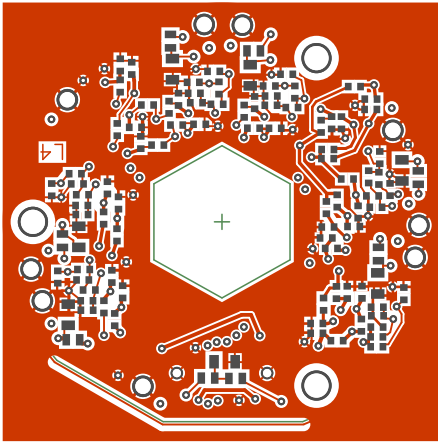


Figure 7: Back layer copper

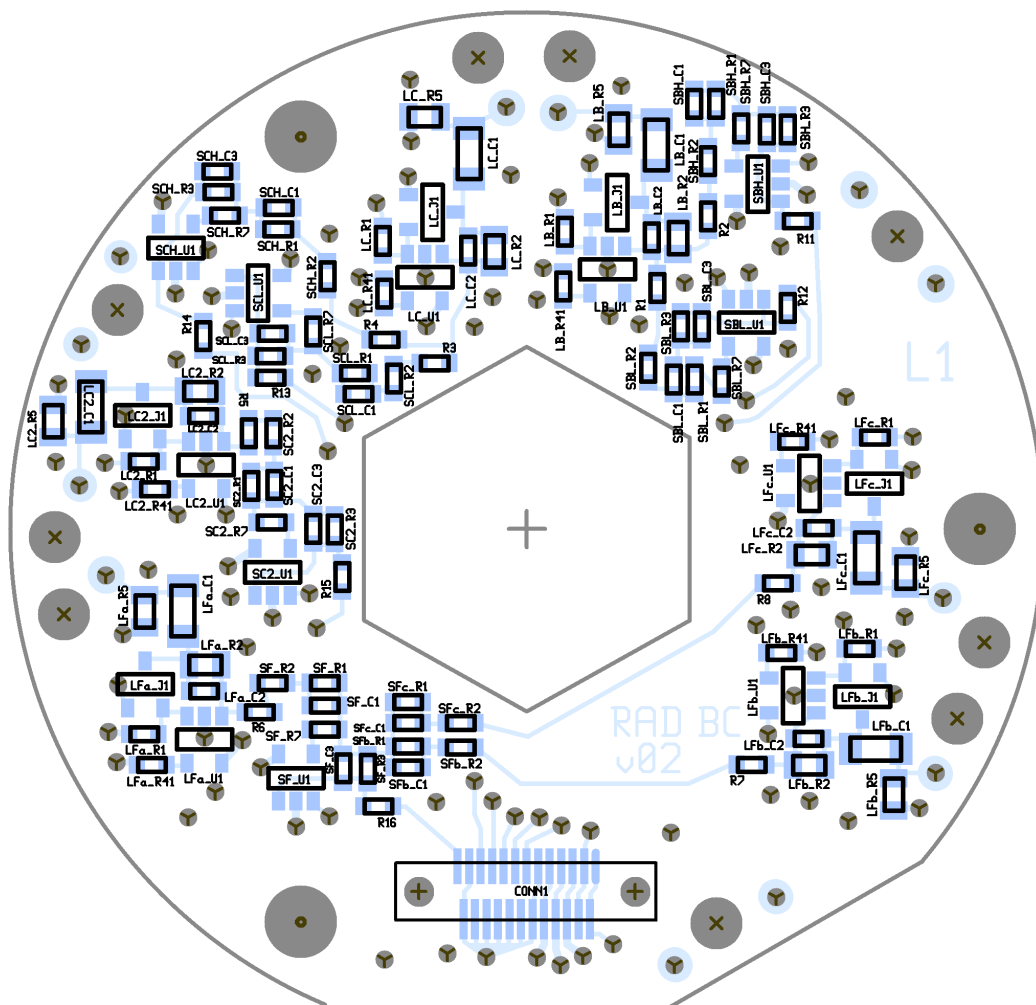


Figure 8: Front layer assembly

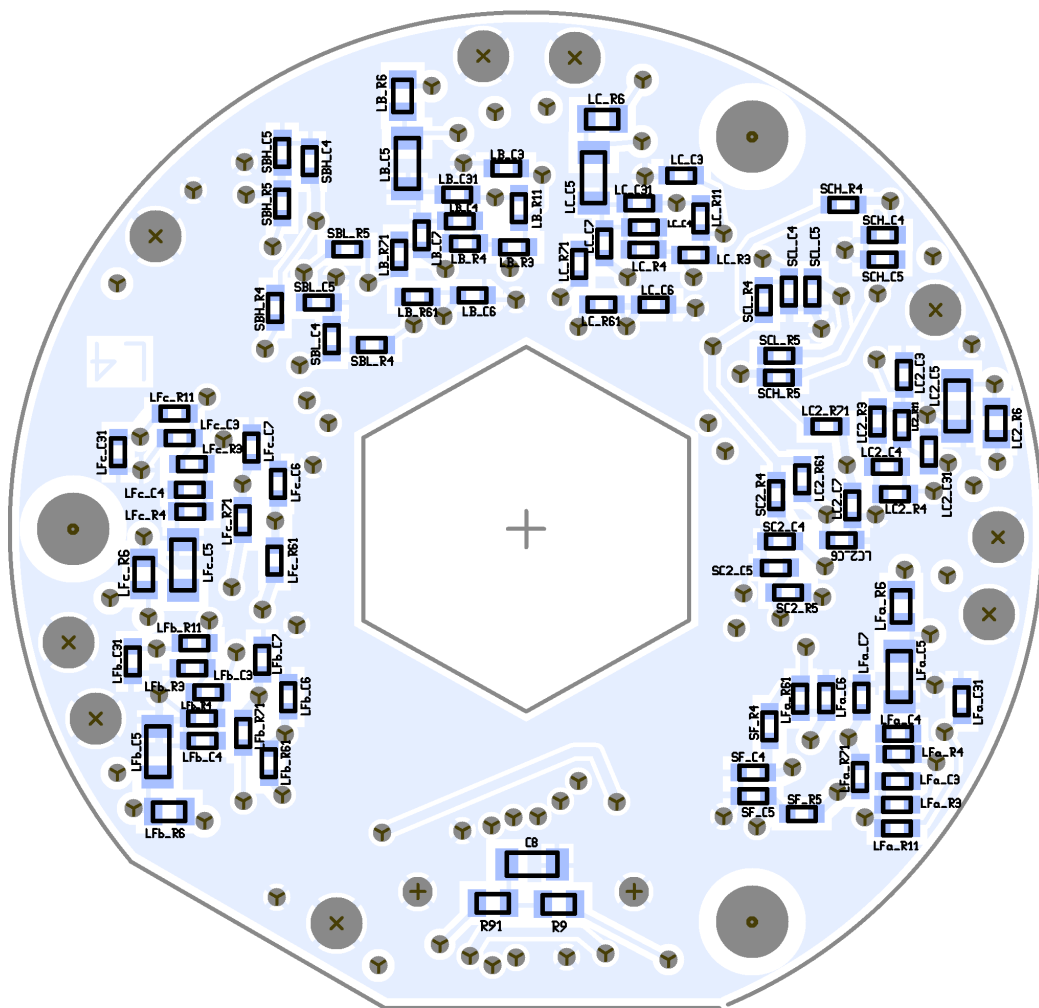


Figure 9: Back layer assembly