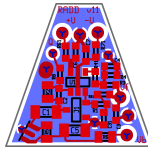


MSL RAD Front-End-Electronics

RADD PCB layout

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The RADD boards supports the readout of the PIN diodes on the CsI scintillator crystal of the RAD instrument, one RADD board for each of three diodes.

The board will be attached to the PIN diode via a small flex strip, which is glued and wire-bonded to the detector.

The power supply of the RADD board comes via Teflon insulated wires (17-strand AWG 32) from the RADE board. The output signal will be connected either via a thin Teflon insulated coax cable (core 7-strand AWG 34) or with twisted pairs of the same type of wires as for the power supply.

The electronics on the RADD board is a *Charge Sensitive Amplifiers* (CSA).

1 Fabrication

The board shall be made according to IPC 6012 class 3 standards.

1.1 Material

The base material is polyimide glass, Total board thickness $0.5\text{ mm} + 0\% - 20\%$, with $35\text{ }\mu\text{m}$ copper thickness, surface finish HAL PbSn, with solder mask on the top side side, *no* silk screens.

1.2 Design Rules

The minimum trace width is 0.2 mm (8 mil), clearance 0.2 mm (8 mil), the clearance on top surfaces to copper carrying -70 V shall be 0.3 mm (12 mil).

The minimum via hole diameter is 0.4 mm (16 mil), with annular rings of at least 0.25 mm (10 mil) width.

1.3 Layers

The board has two copper layers, with SMD components on the top side. The backside is filled with a ground plane.

The ground plane has a cutout under the inverting input node of the current feedback amplifier (AD 8005).

Layer order	Gerber file
1 front layer copper	v11.group0.gbr
2 back layer copper	v11.group1.gbr
board shape	v11.group2.gbr
front solder mask	v11.frontmask.gbr
drill file	v11.plated-drill.cnc
back solder mask	(v11.backmask.gbr)
front solder paste	(v11.frontpaste.gbr)
front silk screen	(v11.frontsilk.gbr)
fab, please ignore	(v11.fab.gbr)

The files in parenthesis are PCB tool output not relevant to this board's fabrication.

1.4 Outline

The board outline is the centerline of the traces on Gerber layer v11.group2.gbr.

2 Design

2.1 Tools

The design is done with GNU EDA tools. (<http://www.geda.seul.org/>)

The layout tool is PCB version 20060822. GAF version is 20060824.

2.2 Schematics

The schematics for the CSA is shown in Fig. 1.

2.3 Layout

Figs. 2 and 3 show the copper layer layouts. Each layer is shown at scale 1:1 and expanded to text width.

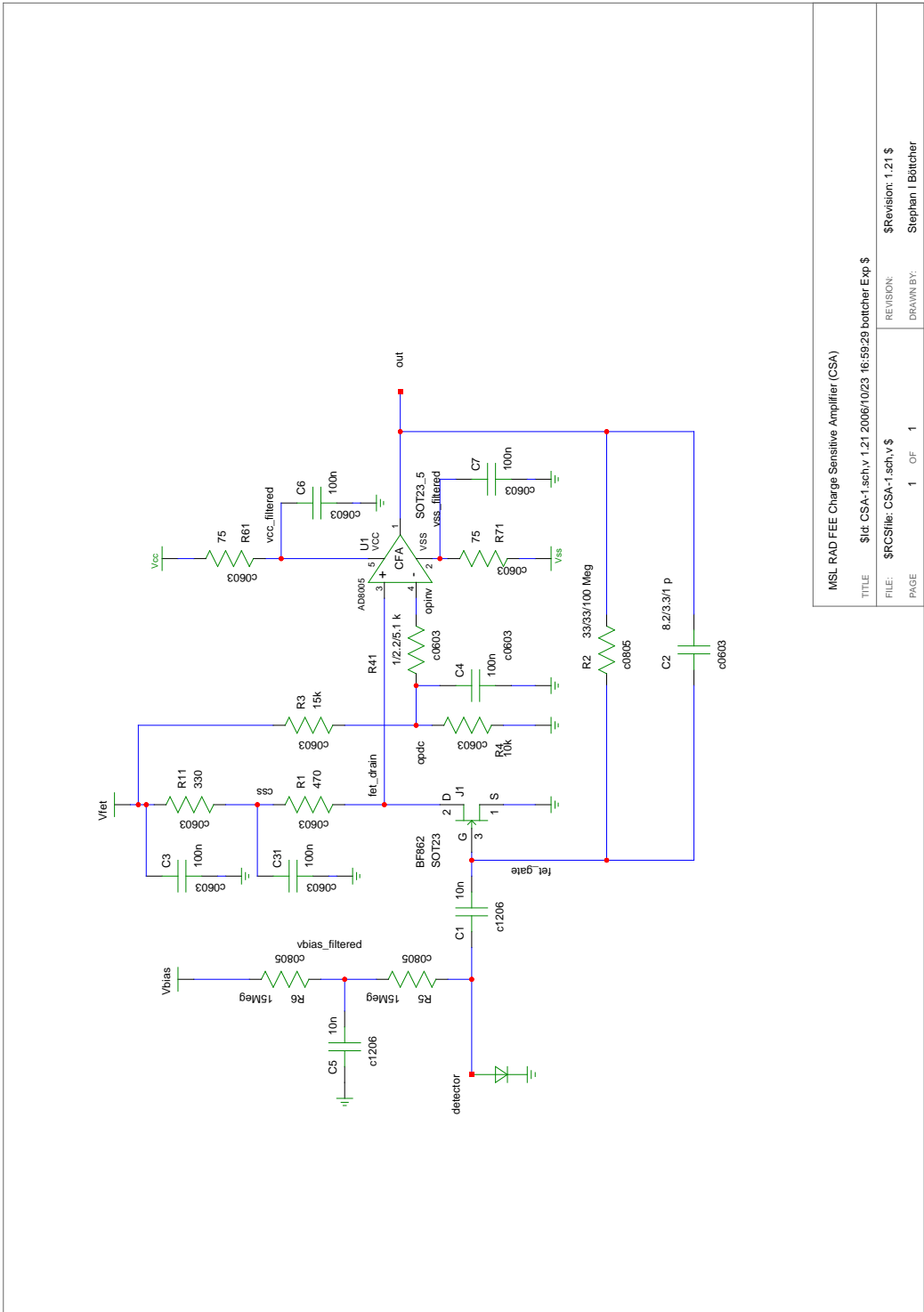


Figure 1: Charge sensitive amplifier schematics: CSA-1.sch

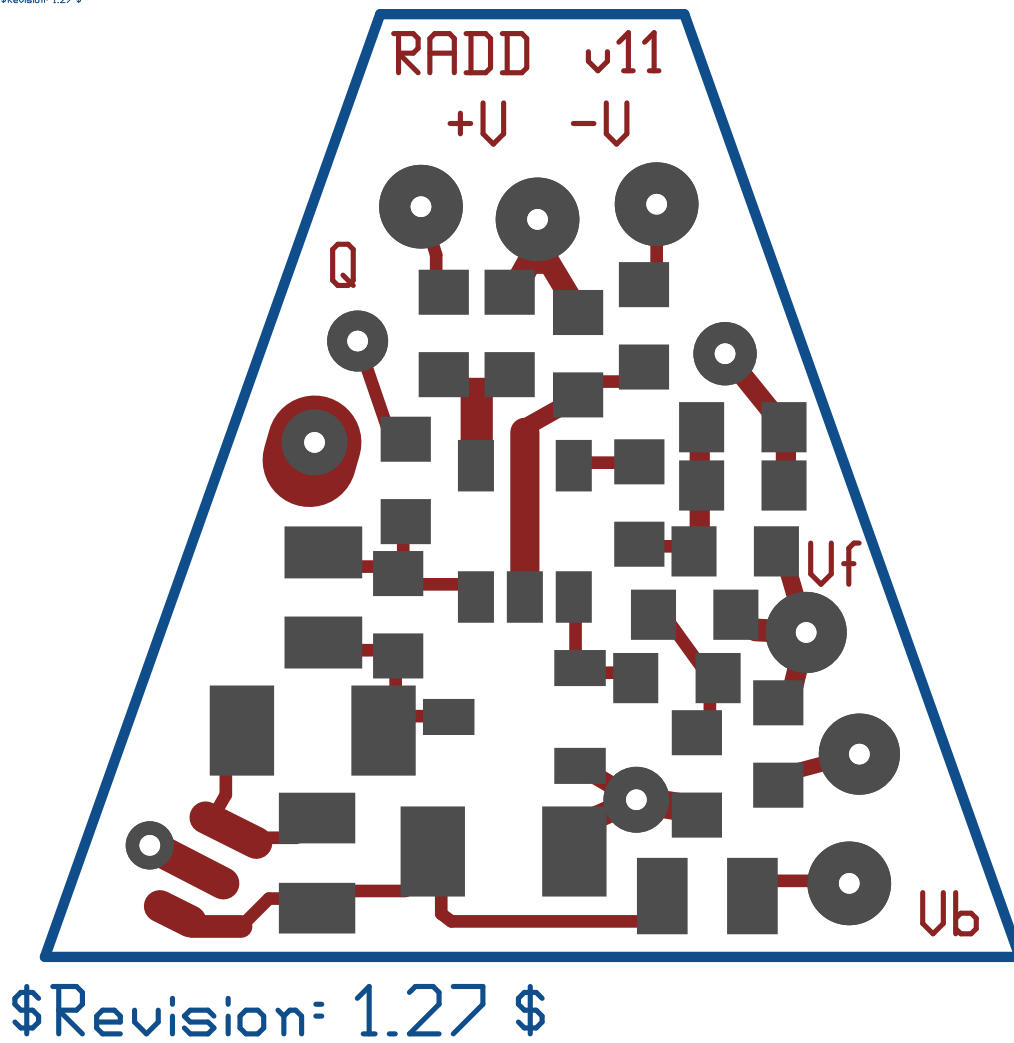
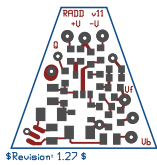
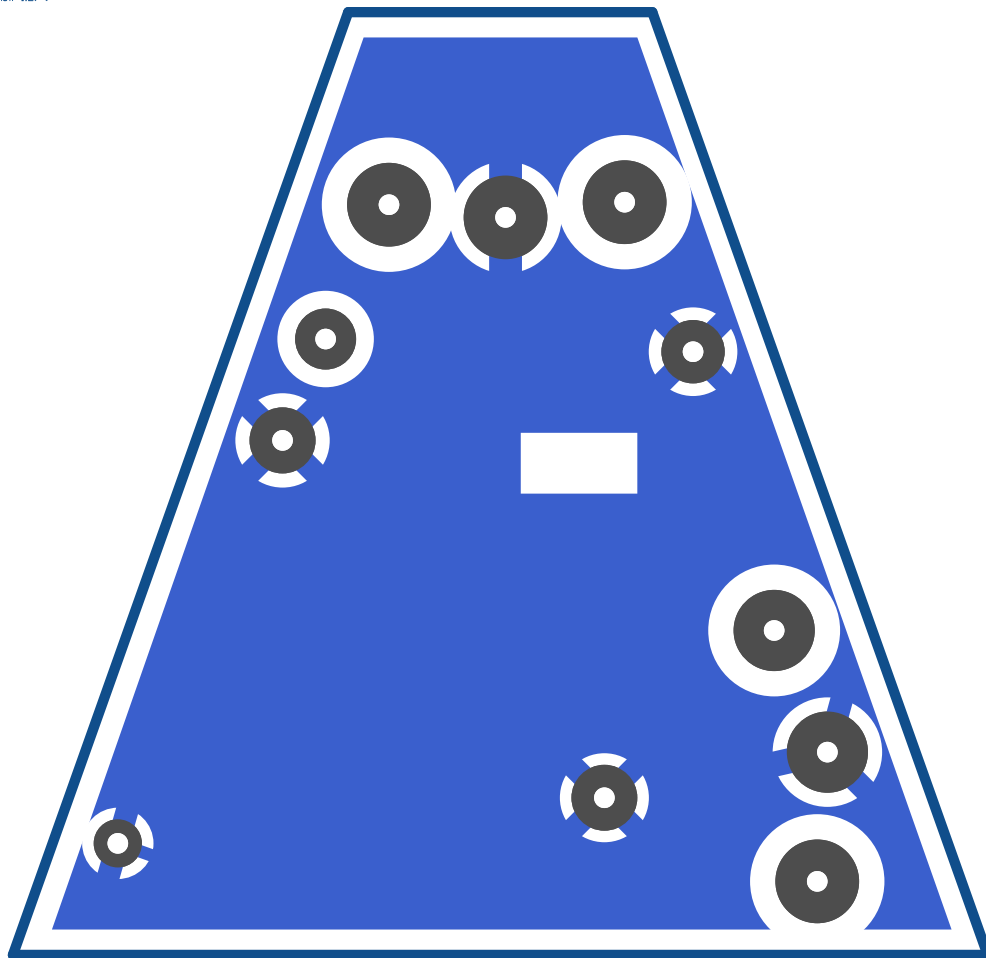
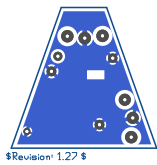


Figure 2: Front layer copper



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Figure 3: Back layer copper

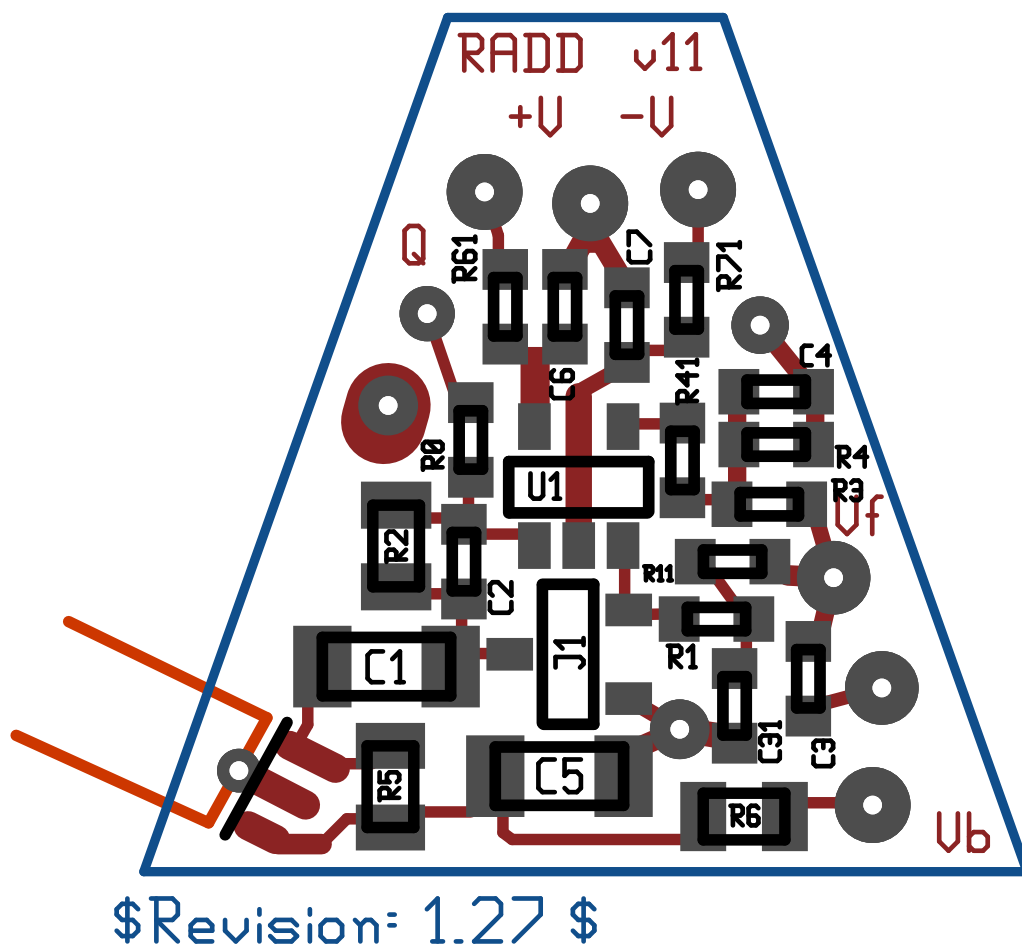


Figure 4: Front layer assembly