# MSL RAD Front-End-Electronics
RADE PCB layout

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v04: December 12, 2006
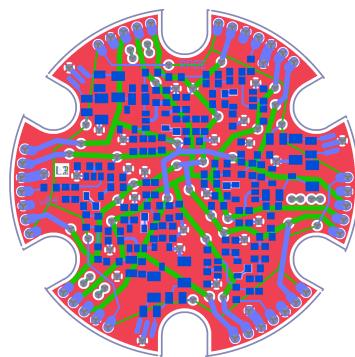
The RADE board supports the readout of the neutron channel scintillator of the RAD instrument.

The board will be mounted below the neutron channel, with the backside facing the scintillator. The board shape is circular with a diameter of 46 mm, with six cutouts to accommodate the inner preload spring assembly. The board shall be staked to the upper spring plate, with a thin insulating layer of polyimide glass between the board and the plate.

Three neutron channel detectors will be connected with small flex strips, which are glued and wire-bonded to the detector. The other end of the strips will be staked to the RADE board and connected with short solder wires.

The power supply of the RADE electronics is routed via Teflon insulated wires (17-strand, AWG 32) from the RADF board through the anticoincidence scintillator to solder pads on the perimeter of the RADE board. A further set of solder pads supports the power supply wires to the RADD boards.

The electronics on the RADE board include three *Charge Sensitive Amplifiers* (CSA) and three *Fast Shapers* (FSH).

1 Fabrication

The board shall be made according to IPC 6012 class 3 standards.

1.1 Material

The base material is polyimide glass, Total board thickness $1\,\mathrm{mm} \pm 10\,\%$, with $35\,\mu\mathrm{m}$ copper thickness, surface finish HAL PbSn, with solder mask on the front side only, *no* silk screens.

1.2 Design Rules

The minimum trace width is $0.2\,\mathrm{mm}$ ($8\,\mathrm{mil}$), clearance $0.2\,\mathrm{mm}$ ($8\,\mathrm{mil}$), the clearance on top surfaces to copper carrying $-70\,\mathrm{V}$ shall be $0.3\,\mathrm{mm}$ ($12\,\mathrm{mil}$).

The minimum via hole diameter is $0.4\,\mathrm{mm}$ ($16\,\mathrm{mil}$), with annular rings of at least $0.25\,\mathrm{mm}$ ($10\,\mathrm{mil}$) width.

The edge clearance of copper traces and pads is $0.5\,\mathrm{mm}$ ($20\,\mathrm{mil}$) minimum.

1.3 Layers

The board has four copper layers, with SMD components on one side. The backside is filled with a ground plane.

The inner layers are a ground plane and a power routing layer. The layer order is front, ground, power, back. The ground plane has cutouts under the inverting input nodes of the current feedback amplifiers (AD 8005).

Layer order		Gerber file
1	front layer copper	`v04.group0.gbr`
2	ground layer copper	`v04.group3.gbr`
3	power layer copper	`v04.group4.gbr`
4	back layer copper	`v04.group1.gbr`
	board shape	`v04.group2.gbr`
	front solder mask	`v04.frontmask.gbr`
	drill file	`v04.plated-drill.cnc`
	back solder mask	`(v04.backmask.gbr)`
	front solder paste	`(v04.frontpaste.gbr)`
	back solder paste	`(v04.backpaste.gbr)`
	front silk screen	`(v04.frontsilk.gbr)`
	back silk screen	`(v04.backsilk.gbr)`
	fab, please ignore	`(v04.fab.gbr)`

The files in parenthesis are PCB tool output not relevant to this board's fabrication.

2 Design

2.1 Tools

The design is done with GNU EDA tools. (`http://www.geda.seul.org/`) The layout tool is PCB version 20060822. GAF version is 20060824.

2.2 Schematics

The schematics for the CSA and FSH were derived from master schematics (Fig. 2 and 3) by a script which prefixes net names and reference designators with an instance prefix, `L1_`, `L2_`, and `L3_` for the CSAs, and `S1_`, `S2_`, and `S3_` for the shapers. The RADE schematics (Fig. 1) defines connections between the amplifier instances, and to the solder pads.

2.3 Layout

Fig. 4 to 7 show the copper layer layouts, Fig. 8 shows the silk layer (not to be printed on the board).

Each layer is shown at scale 1:1 and expanded to text width.

refdes=CONN
footprint=RADE

net=Vcc:1
net=Vss:2
net=vfet:3
net=GND:4
net=vbias:5
net=vfet:6
net=Vss:7
net=GND:8
net=E3:9
net=GND:10
net=Vcc:11
net=vbias:12
net=Vcc:13
net=Vss:14
net=vfet:15
net=GND:16
net=vbias:17
net=vfet:18
net=Vss:19
net=GND:20
net=E2:21
net=GND:22
net=Vcc:23
net=vbias:24
net=Vcc:25
net=Vss:26
net=vfet:27
net=GND:28
net=vbias:29
net=vfet:30
net=Vss:31
net=GND:32
net=E1:33
net=GND:34
net=Vcc:35
net=vbias:36
net=GND:37
net=GND:38
net=GND:39

E1
R1
c0603
47
S1_out

E2
R2
c0603
47
S2_out

E3
R3
c0603
47
S3_out

R4
c0603
1.62k
S1_in
L1_out

R5
c0603
330
S2_in
L2_out

R6
c0603
220
S3_in
L3_out

MSL RAD FEE: RADE board interconnects

TITLE	$Id: RADE.sch,v 1.6 2006/11/07 12:20:04 bottcher Exp $	
FILE:	$RCSfile: RADE.sch,v $	REVISION: $Revision: 1.6 $
PAGE	1 OF 1	DRAWN BY: Stephan l Böttcher

Figure 1: RADE master schematics: `RADE.sch`
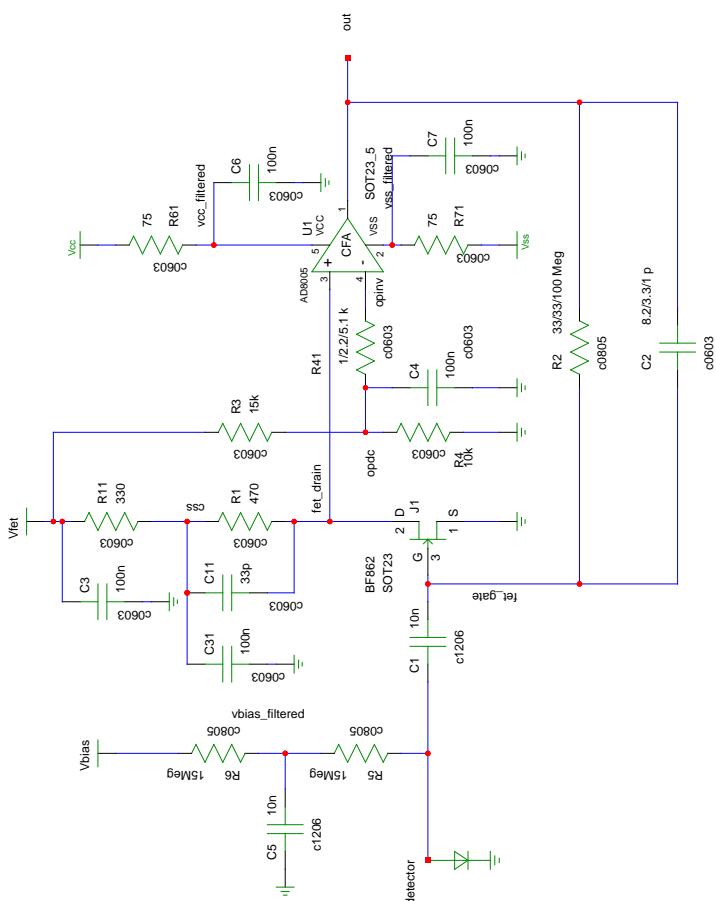
Figure 2: Charge sensitive amplifier schematics: `CSA-1.sch`
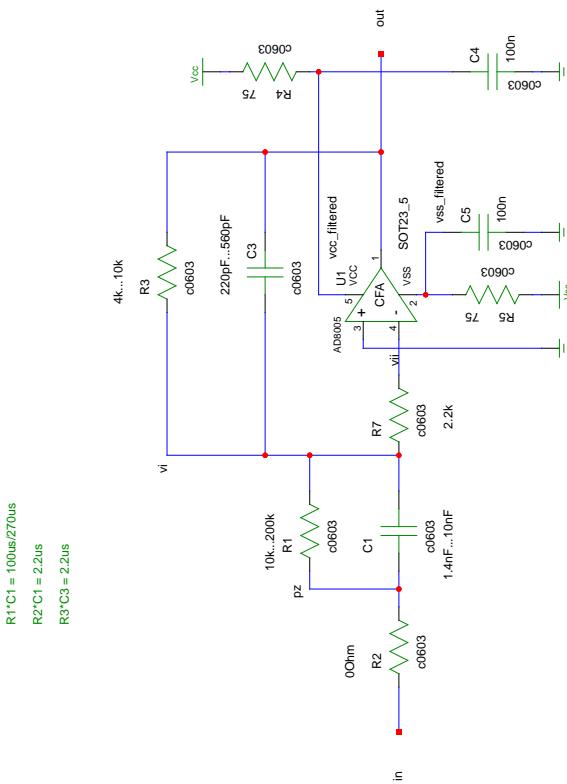
Figure 3: Fast shaper schematics: `FSH-1.sch`

RADE v04 $Revision: 1.22 $
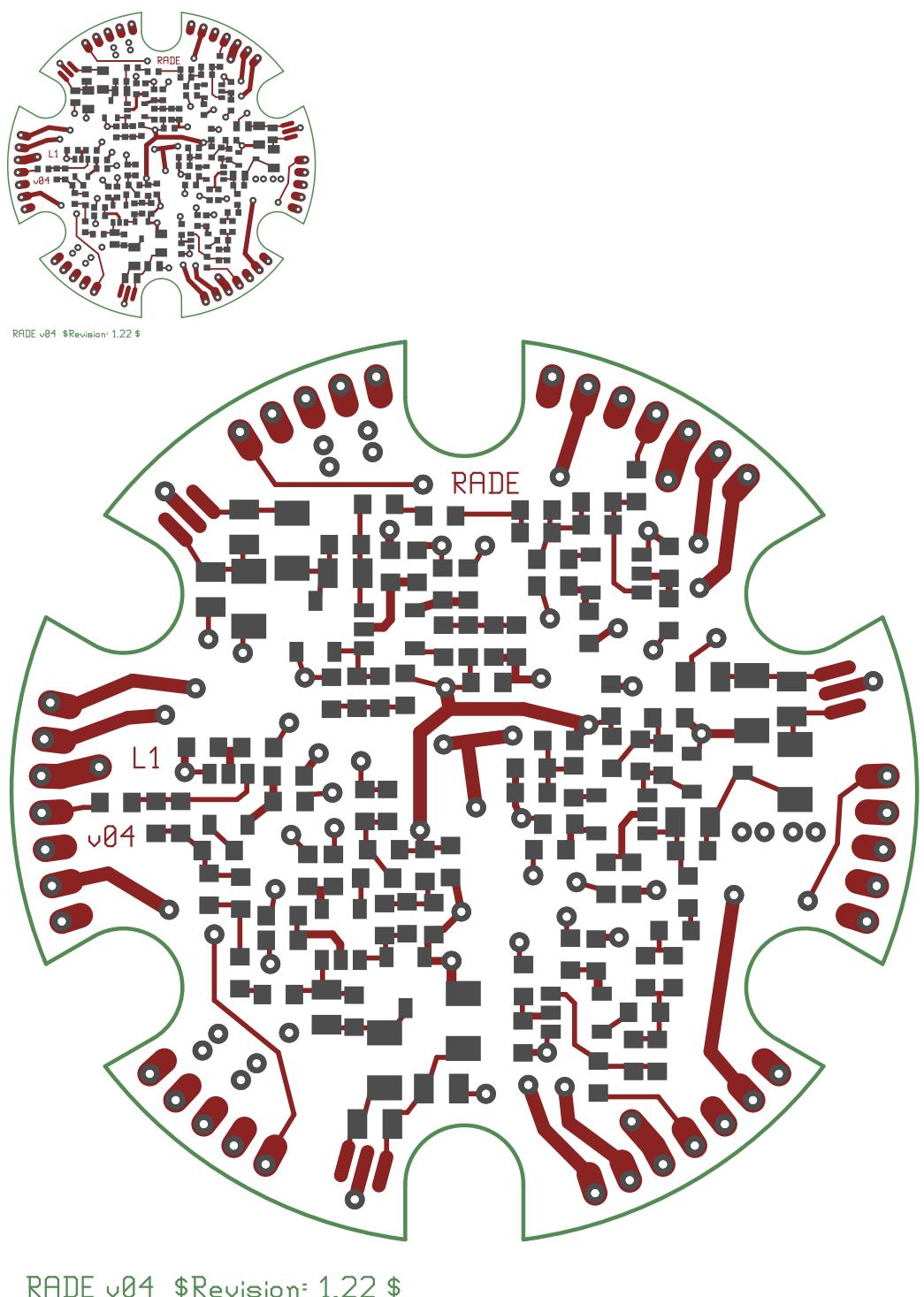
Figure 4: Front layer copper

Figure 5: Ground layer copper

Figure 6: Power layer copper
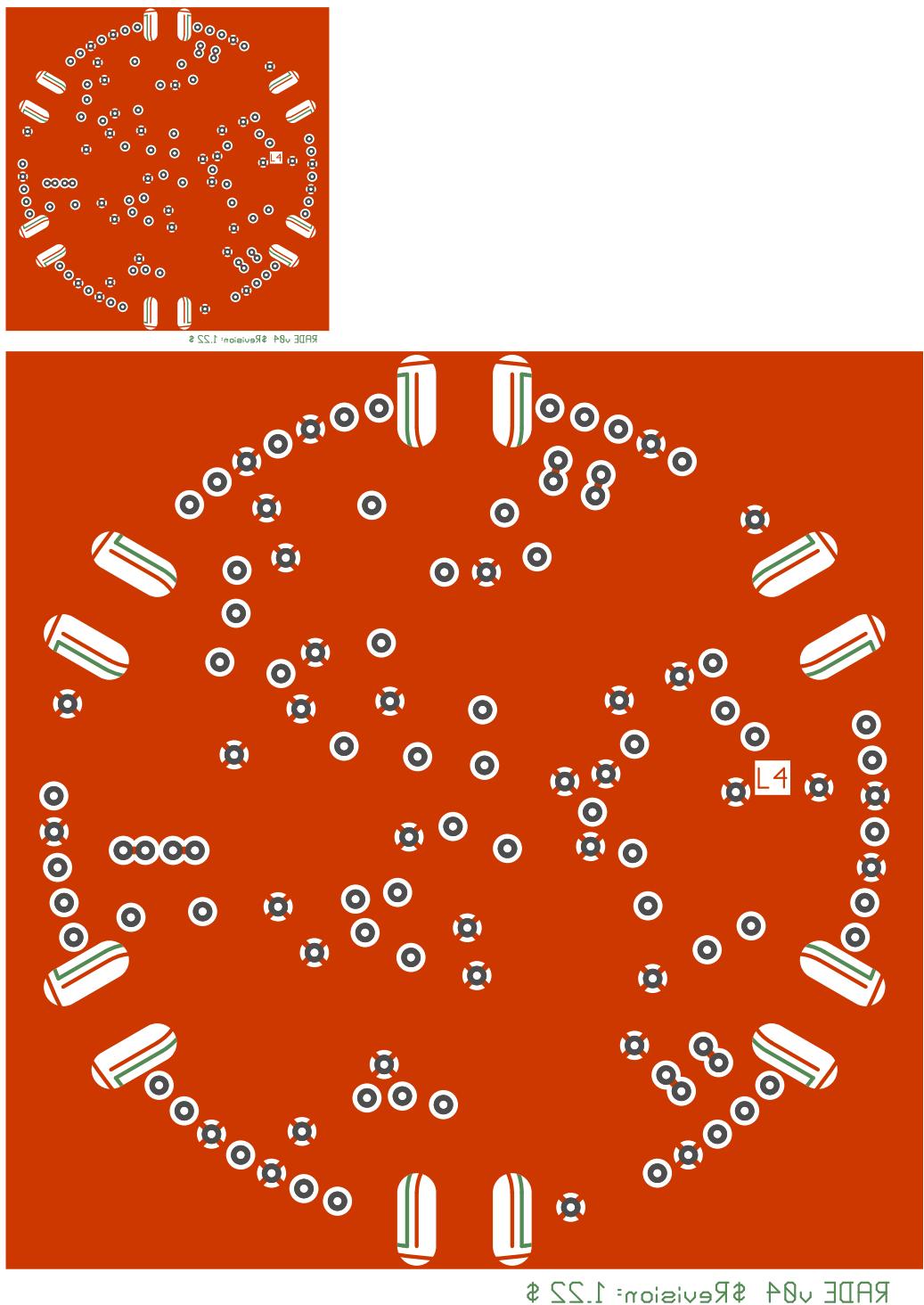
Figure 7: Back layer copper

Figure 8: Assembly