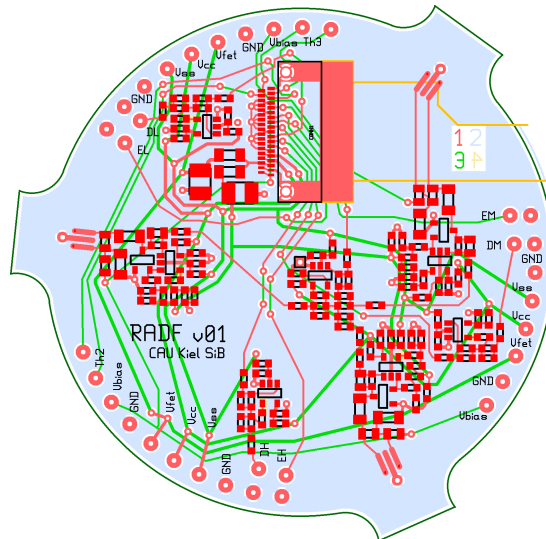


MSL RAD Front-End-Electronics

RADF PCB layout

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The RADF board supports the bottom readout of the anticoincidence scintillator of the RAD instrument, signal shaping for the CsI readout, and power distribution for all the bottom part of the instrument.

The board will be mounted below the anticoincidence detector, with the backside facing the scintillator. The board shape is circular with a diameter of 67 mm, with three protrusions going between the outer spring assembly, to accommodate the detector contacts. The board shall be staked to the upper spring plate, with a thin insulating layer of polyimide glass between the board and the plate.

Three anticoincidence channel detectors will be connected with small flex strips, which are glued and wire-bonded to the detector. The other end of the strips will be staked to the RADF board and connected with short solder wires.

The downstream connections to the TFlex goes through a horizontal surface mount Omnetics connector. The upstream power supply and thermistor connections of calorimeter are routed via Teflon insulated wires (19-strand, AWG 32) from solder pads on the perimeter of the RADF board through the anticoincidence scintillator to solder pads on the perimeter of the RADE board. The detector signals from the calorimeter channels reach the RADF board via coax wires terminating on pairs of solder pads on the perimeter of the board.

The electronics on the RADF board include three *Charge Sensitive Amplifiers* (CSA) and one *Fast Shaper* (FSH) for the anticoincidence readout, three more Fast Shapers for the CsI readout, two FET bias filters, and a connector.

1 Fabrication

The board shall be made according to IPC 6012 class III standards.

1.1 Material

The base material is polyimide glass, Total board thickness $1\text{ mm} \pm 10\%$, with $35\text{ }\mu\text{m}$ copper thickness, surface finish HAL PbSn, with solder mask and silk on the front side only.

1.2 Design Rules

The minimum trace width is 0.2 mm (8 mil), clearance 0.2 mm (8 mil), the clearance on top surfaces to copper carrying -70 V shall be 0.3 mm (12 mil).

The minimum via hole diameter is 0.4 mm (16 mil), with annular rings of at least 0.25 mm (10 mil) width.

The edge clearance of copper traces and pads is 0.5 mm (20 mil) minimum.

1.3 Layers

The board has four copper layers, with SMD components on one side. The backside is filled with a ground plane.

The inner layers are a ground plane and a power routing layer. The layer order is front, ground, power, back. The ground plane has cutouts under the inverting input nodes of the current feedback amplifiers (AD 8005).

Layer order	Gerber file
1 front layer copper	v01s.group0.gbr
2 ground layer copper	v01s.group1.gbr
3 power layer copper	v01s.group2.gbr
4 back layer copper	v01s.group3.gbr
board shape	v01s.group4.gbr
front solder mask	v01s.frontmask.gbr
front silk screen	v01s.frontsilk.gbr
drill file	v01s.plated-drill1.cnc
back solder mask	(v01s.backmask.gbr)
front solder paste	(v01s.frontpaste.gbr)
fab, please ignore	(v01s.fab.gbr)

The files in parenthesis are PCB tool output not relevant to this board's fabrication.

2 Design

2.1 Tools

The design is done with GNU EDA tools. (<http://www.geda.seul.org/>)
The layout tool is PCB version 20060822. GAF version is 20060824.

2.2 Schematics

The schematics for the CSA and FSH were derived from master schematics (Fig. 2 and 3) by a script which prefixes net names and reference designators with an instance prefix, **LFa**_, **LFb**_, and **LFc**_ for the CSAs, and **SF**_, **SDH**_, **SDM**_, and **SDL**_ for the shapers. The RADF schematics (Fig. 1) defines connections between the amplifier instances, connector, and to the solder pads.

2.3 Layout

Fig. 4 to 7 show the copper layer layouts, Fig. 8 shows the reference designators of all parts.

Each layer is shown at scale 1:1 and expanded to text width.

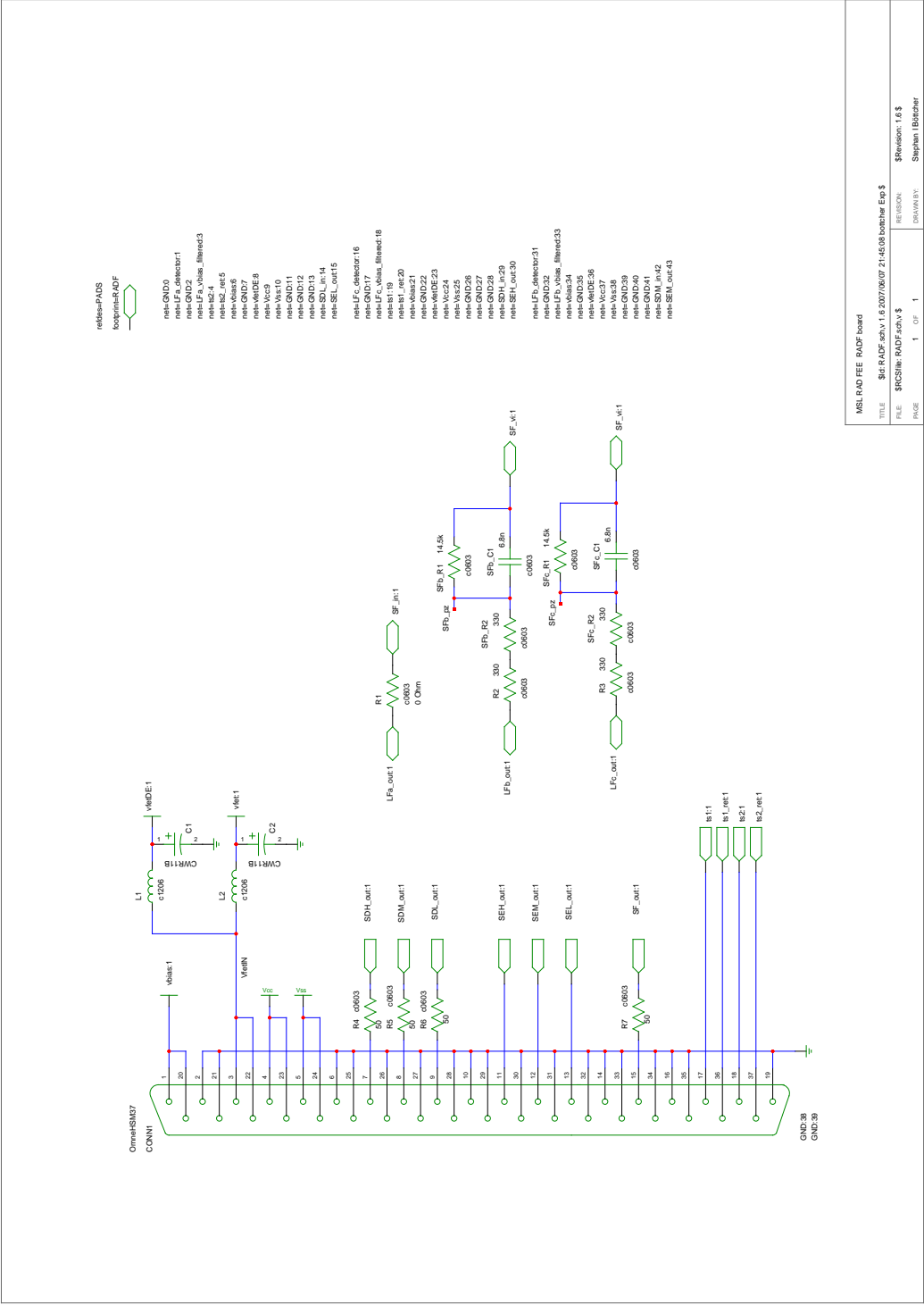
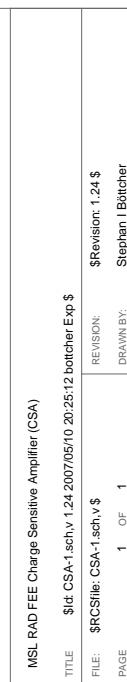


Figure 1: RADF master schematics: RADF.sch



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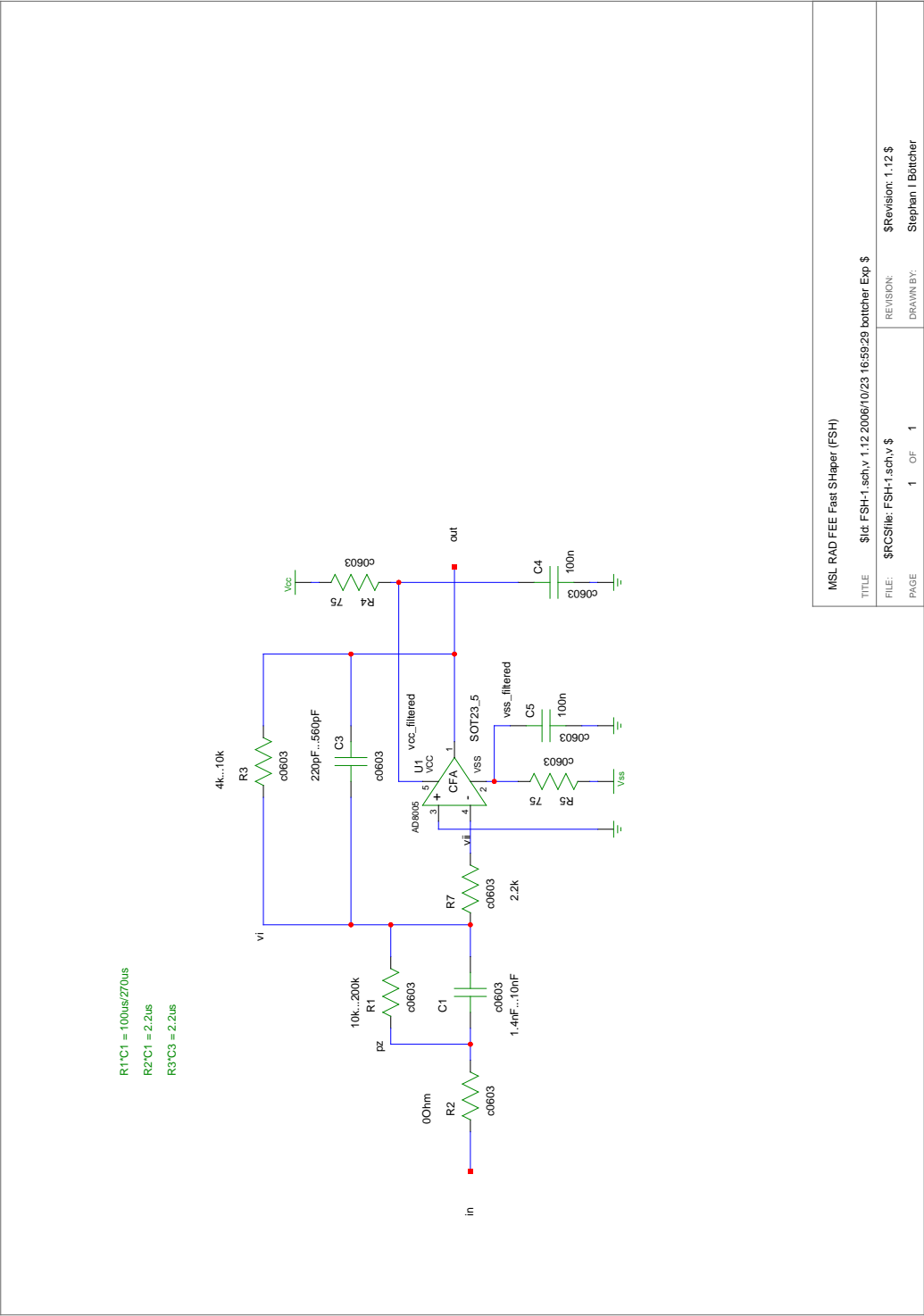


Figure 3: Fast shaper schematics: FSH-1.sch

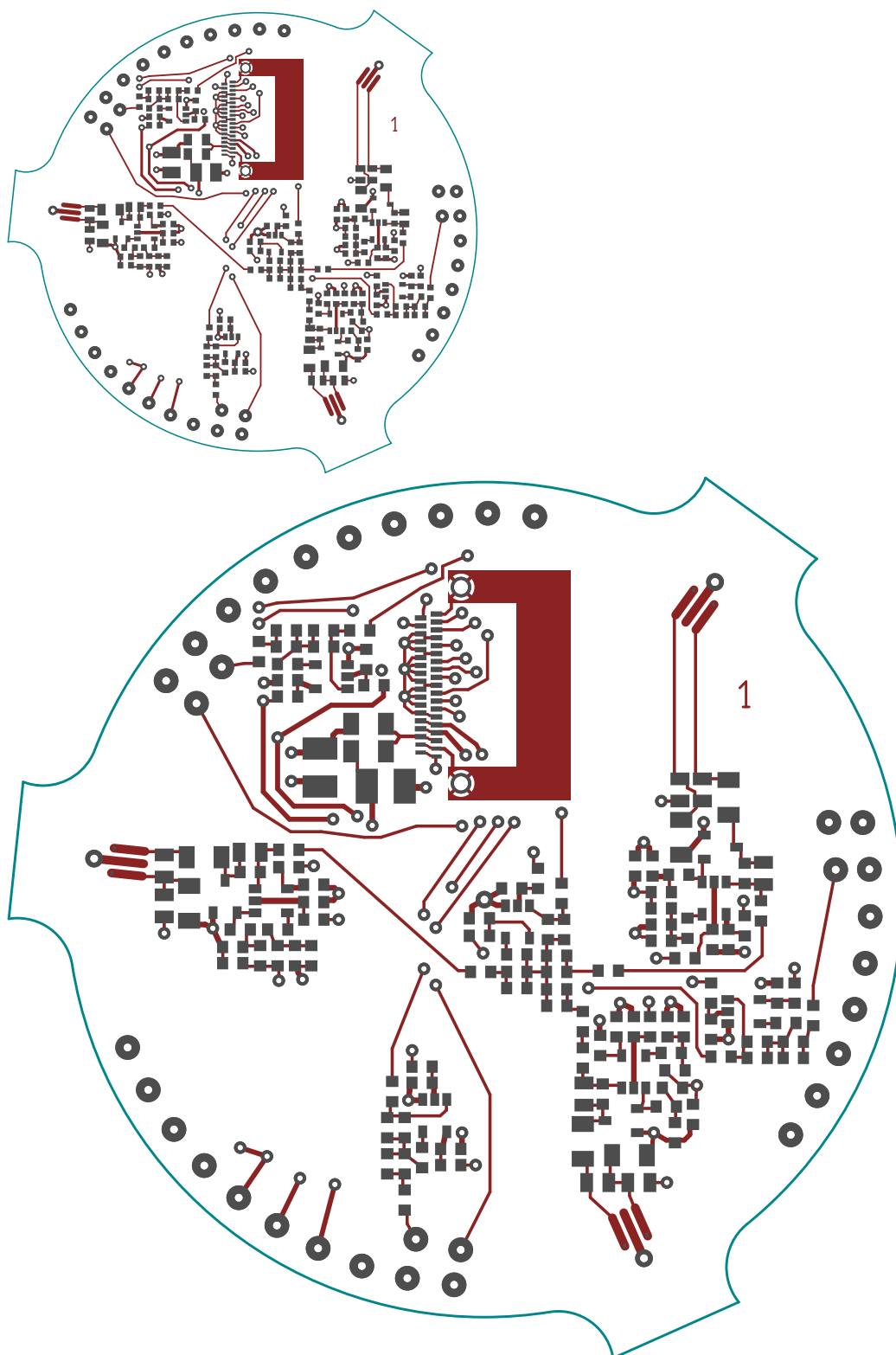


Figure 4: Front layer.

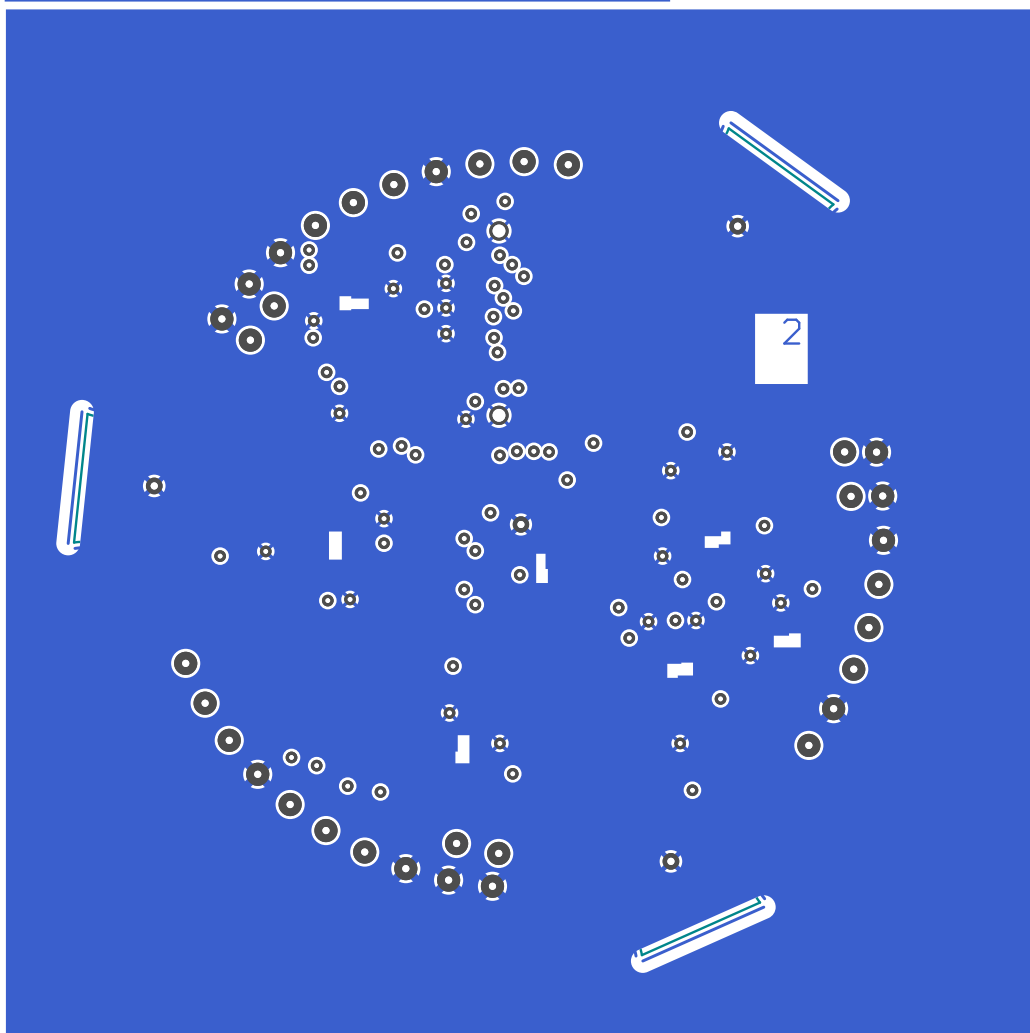
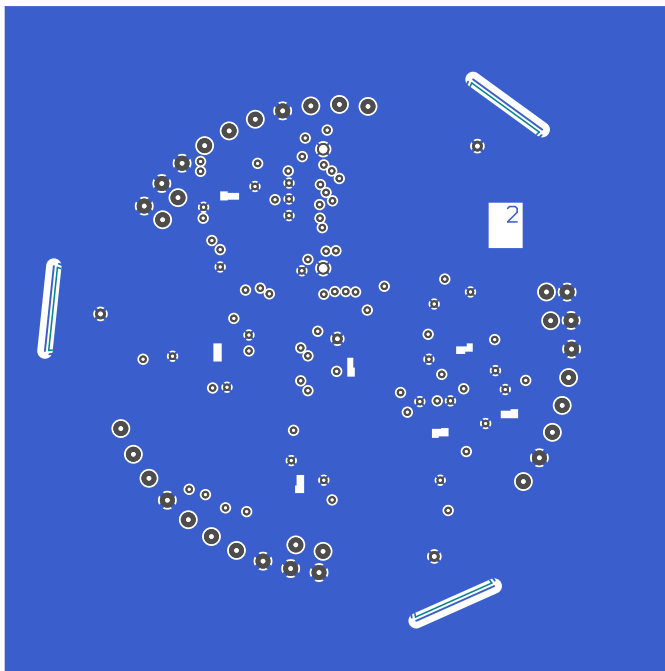


Figure 5: Ground layer.

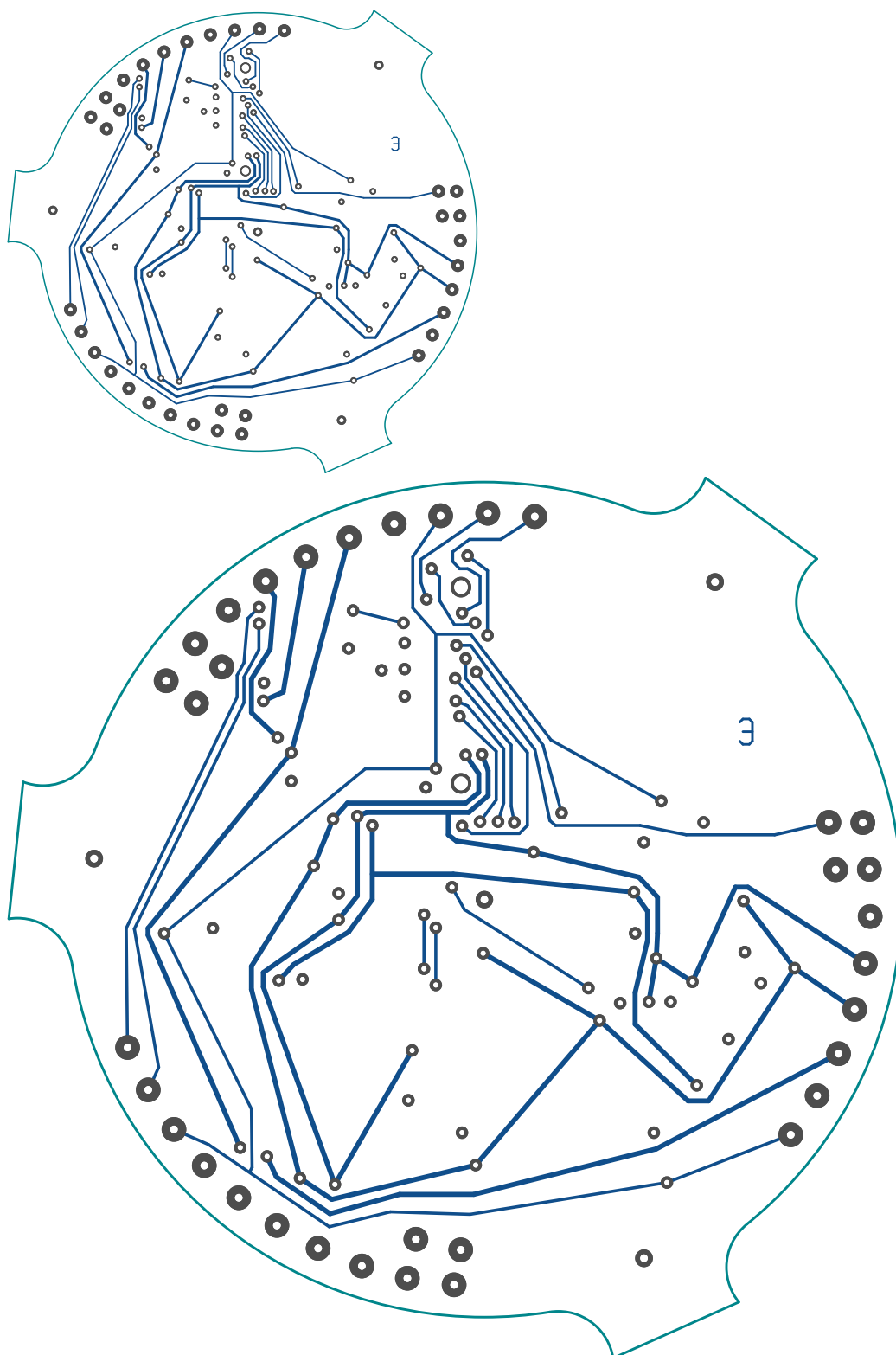


Figure 6: Power layer.

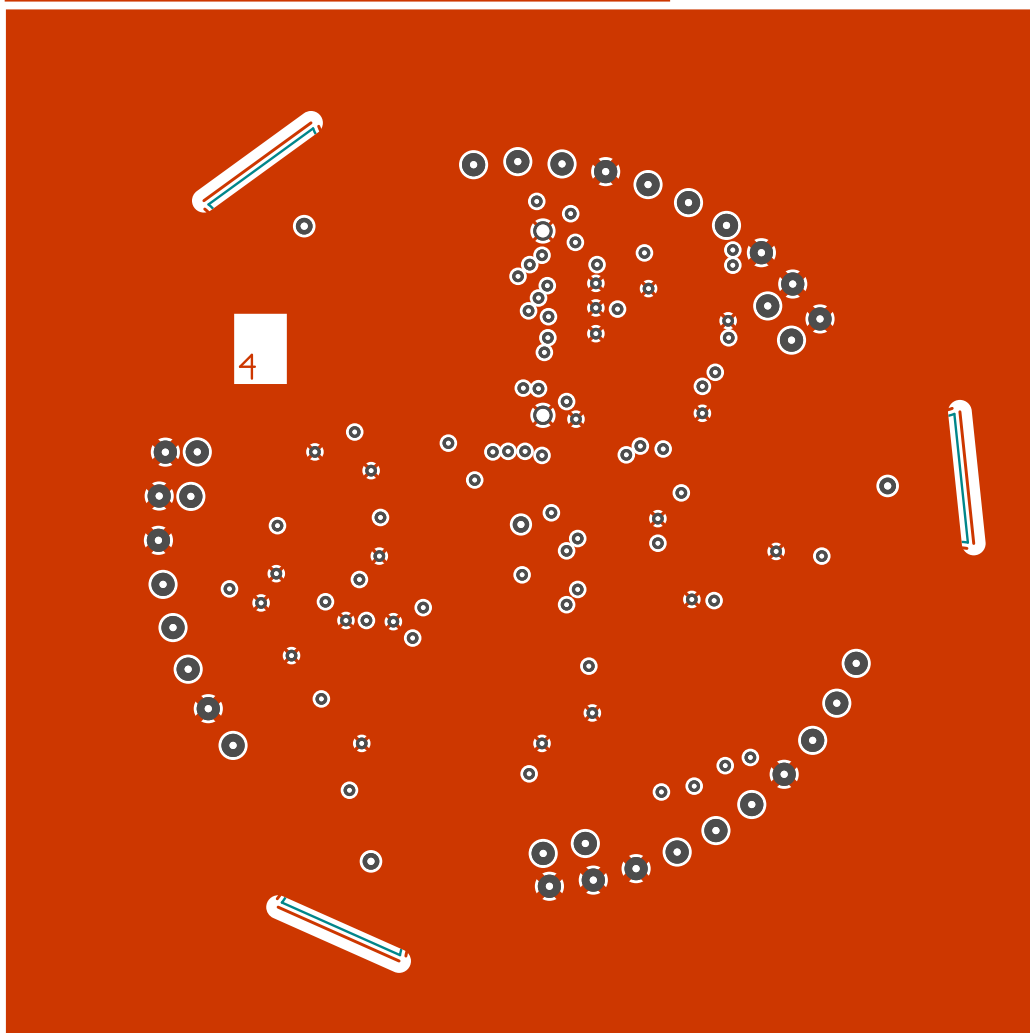
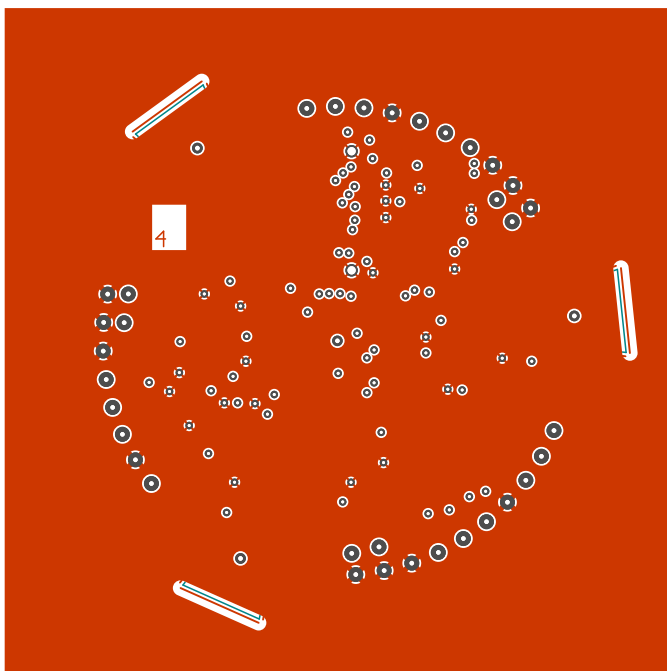


Figure 7: Back layer.

